ABSTRACT

This manual describes the installation, programming, operation and maintenance of the Ball Computer Products 3120 Tape Controller for Wangco and Pertec NRZI magnetic tape drives.

3120 TAPE CONTROLLER
TECHNICAL MANUAL

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SECTION 1
GENERAL INFORMATION

1.1 SCOPE

This manual describes the Ball Computer Products (BCP) 3120 Tape Controller for Wangco and Pertec NRZI magnetic tape drives. Section 1 presents introductory information and specifications, Section 2 describes installation requirements and Section 3 outlines the controller's programming conventions. Section 4 describes the theory of operation while Section 5 presents maintenance information and includes a complete electronic parts list. Section 6 includes all schematic diagrams and related drawings. The manual is concluded with a series of appendices describing interface requirements for specific drive manufacturers and models.

1.2 INTRODUCTION

The 3120 Tape Controller is designed to interface any of the Data General Nova or Digital Computer Controls D-116 series minicomputers with up to four Wangco or Pertec dual-gap magnetic tape drives. The controller is compatible with both IBM standard seven-track and ANSI standard nine-track formats and can support a mixture of both seven- and nine-track drives within the same system. A unique three-character packing mode is additionally available to seven-track drives. The controller supports standard drive speeds ranging from 12.5 to 75 inches per second (ips).

The controller features program selection of odd or even parity, character densities of either 800 or 556 characters per inch (cpi) on seven-track drives with the dual-density option and an edit feature optionally avialable with some drives.

During operation, the controller performs vertical parity checks on each character and a longitudinal redundancy check of each track at the conclusion of a record. In the nine-track mode, a CRC (Cyclic Redundancy Check) character is additionally written at the conclusion of each record and can

be read back into core using the "diagnostic mode". The controller utilizes the CPU's data (DMA) channel to transfer information and is capable of transferring up to 32K of words using only three instructions.

The controller includes an I/O adapter board for interfacing directly to the selected tape drive, all necessary interface cables, a tape exerciser program and software input and output drivers compatible with BCP's Decision Disk Operating System (DDOS).

The 3120 Controller can be combined with the BCP 3180 PE Tape Controller (3180/20 option) to provide compatibility with PE/NRZI dual-format drives. In this configuration, the two controllers share a common bus between all drives, permitting program selection of the recording format.

1.3 SPECIFICATIONS

Specifications for the 3120 Tape Controller are listed in the following table (Table 1-1).

TABLE 1-1
SPECIFICATIONS

COMPATIBILITY	
CPU	Any Data General Nova or Digital Computer Controls D-116 series minicomputer.
Tape Drives	Wangco series 7, 8, 10 and 11 and Pertec series 5000, 6000, 7000 and T8000 NRZI seven- or nine-track drives with dual-gap heads. Up to four drives may be interfaced to a controller via a "daisy-chain" technique, provided all drives are from the same manufacturer and operate at the same tape speed. Comparable drives from other manufacturers can additionally be supported.

TABLE 1-1 (Continued)

TAPE FORMAT	
Tape	Computer grade, 0.5 inch wide ANSI standard with reflective BOT and EOT markers.
Density	Nine-track: 800 characters per inch (cpi) Seven-track: 800 or 556 cpi Dual-density (800/556 cpi) drives are supported with the desired recording density selectable through the program.
Format	IBM standard seven-track or ANSI standard nine-track NRZI formats (program selectable).
Data Packing	Controller arranges 16-bit data word into two tape characters. Unique three-character mode available with seven-track drives (program selectable).
Speed	12.5, 15, 25, 37.5, 45 or 75 inches per second (ips). Tape speed supported specified at time of manufacture (may be field altered).
Parity	Odd parity. Vertical parity across a character written and verified on all drives. As a diagnostic aid, even parity is available (program selectable).
PHYSICAL	
Dimensions	Logic card: 15" x 15" x 1/2" (LxWxH) I/O Adapter Card: 7" x 5.2" (LxW)
Weight	Logic card: 40 oz (net) I/O Adapter card: 14 oz (net) Shipping: 8 lbs.
Power	5 (±0.2) volts at 4.5 amperes, supplied from Nova back panel.

TABLE 1-1 (Continued)

Environmental	Surpasses Nova temperature and humidity specifications.
ACCESSORIES SUPPLIED	
Hardware	3120 Tape Controller logic card I/O Adapter assembly and mounting hardware Two (2) 10-foot controller-to-adapter interface cables 3120 Tape Controller Technical Manual Connector extractor tool (3M No. 3438)
Software	3120 Tape Exerciser manual and binary tape DDOS Magnetic Tape Drivers manual and binary tapes
Documentation and software are normally only supplied initially under OEM agreements.	
OPTIONS	
3180/20 Option	Provides compatibility for NRZI/PE dual-format drives. Option includes the 3120 Controller and a 3180 PE Tape Controller with special common controller-to-adapter interface cables.

SECTION 2
INSTALLATION

2.1 INTRODUCTION

This section describes unpacking, inspection and installation procedures for the 3120 Tape Controller.

2.2 UNPACKING AND INSPECTION

Upon receipt of the controller from the carrier, inspect the two shipping cartons for external damage incurred during transit. Any indication of such damage must be noted by both the carrier and customer and should be reported to the insurance investigator immediately. Carefully unpack the shipping cartons and verify that the following items are included. The packaging material should be retained in case it should become necessary to reship the equipment at a later date.

Item 1: 3120 Tape Controller logic card
Item 2: I/O Adapter assembly and mounting hardware
Item 3: Two (2) controller-to-adapter interface cables.
Item 4: Connector extractor tool (3M No. 3438)
Item 5: Documentation package including:
- 3120 Tape Controller Technical Manual
- 3120 Tape Exerciser manual and binary tape
- DDOS Magnetic Tape Drivers manual and binary tapes

Note: The contents of the documentation package varies with the recipient. Software items are normally supplied only initially with controllers shipped under OEM contracts.

Visually inspect each item for obvious physical damage. Verify that all items specified on both the purchase order and packing slip are included. If any items are missing or damaged, immediately contact the BCP Field Service Representative or the factory.

2.3 REPACKING FOR SHIPMENT

If it should become necessary to return the equipment, contact your local BCP Field Service Representative or the BCP Field Service Department for shipping authorization. If possible, use the original packaging materials. If not available, the equipment should be packaged as follows:

1. Seal the logic card and adapter assembly in dust-proof, moisture-proof plastic bags.
2. To prevent damage in shipment, insulate the equipment with a type of cushioned-packing material, (e.g., convoluted foam or Air-gap®).
3. Place the equipment in reinforced corrugated cartons and seal with strong packing tape.

2.4 SLIDE-MOUNTED RACK PREPARATION

If the CPU is to be mounted in a standard RETMA rack on chassis slides, the right-side rack rail should be modified to prevent possible abrasion of the controller's input/output cables when the computer is slid in or out of the enclosure. Figure 2-1 illustrates the suggested sections to be removed for both the 5-1/4" and 10-1/2" computer configurations. If the rack rails are removable, remove the right-side rail (as viewed from the front of the enclosure) and cut out the designated area. If the rails are an integral part of the enclosure, remove or adequately protect the equipment before cutting out the specified section. Deburr or file all rough edges. To permit ajustment of the slide rails from the front of the enclosure, enlarge the four holes (designated "A") and the corresponding holes on the left rack rail using a 7/32" drill bit.

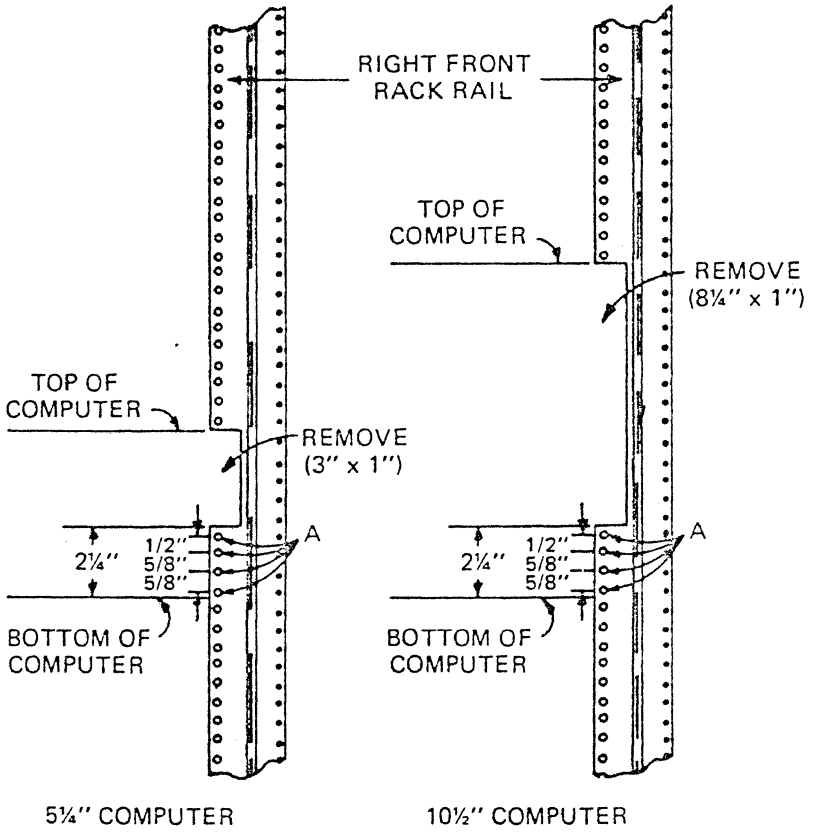


FIGURE 2-1
RACK RAIL MODIFICATION

2.5 INSTALLATION

Installation of the 3120 Controller involves installing the logic card into the CPU, installing the adapter assembly on/into the tape drive, interfacing the logic card to the adapter assembly and interfacing the adapter assembly to the tape drive. Before proceeding, ensure that primary power is removed from both the CPU and tape drive. If the CPU has already been installed in the rack enclosure, slide the CPU out (if equipped with rack slides) or remove the CPU from the enclosure.

2.5.1 Logic Card

The logic card is designed to install directly into any I/O subassembly slot. Unless the system uses another fast peripheral device such as a magnetic disk, A/D interface or high-speed communications interface, the 3120 logic card should occupy the highest priority I/O slot available (slot 3). Since the logic card utilizes the CPU's power supply, the additional current requirement should be considered in regard to the logic card's placement when dual power supplies are available (Nova Jumbos and DCC 116-E).

If, with the selection of the I/O slot, a vacant slot or slots exist between the board located immediately below the logic card and the selected logic card slot, the DCHP (Data CHannel Priority) and INTP (INTerrupt Priority) signals must be physically jumpered on the back panel to maintain interrupt priority. The back panel is accessible from the left side of the CPU. Referring to the "Back Panel Connector Layout" illustration in Appendix A of the Nova manual or the "I/O Signals on Backplane Connector Panel Pins" illustration in Section 10 of the D-116 handbook, install one end of a wire-wrap jumper to the $\overline{\text{DCHP-OUT}}$ signal at pin 93 of the "A" connector (nearest the rear of the CPU) occupied by the device immediately below the logic card. Connect the remaining end of the jumper to the $\overline{\text{DCHP-IN}}$ signal at pin 94 of the "A" connector occupied by the logic card, bridging the vacant slot or slots. Similarly, connect the $\overline{\text{INTP-OUT}}$ signal (pin A95) from the lower device to the $\overline{\text{INTP-IN}}$ signal at pin 96 of the logic card's corresponding "A" connector. This will complete the priority interrupt continuity to the logic card. If vacant I/O slots exist between the logic card and the device above the logic card, perform similar strapping of the DCHP and INTP signals.

2.5.2 Logic Card Configuration

The 3120 logic card includes a number of field-alterable links and components which determine the controller's compatibility with the characteristics of the drive to be interfaced. Normally, drive configuration is specified at the time of purchase and the appropriate links and timing components are installed at the factory prior to shipment.

Note: When the drive characteristics are not specified, the controller will be configured for a 25 ips Wanco 9-track drive.

The following subsections describe the drive configurations supported and the corresponding link positions and component values. If the controller's configuration is to be modified, remove the fiberglass protective cover by extracting the three screws securing the cover in place.

2.5.2.1 Speed Selection

The 3120 Controller supports tape speeds of 12.5, 15, 25, 37.5, 45 and 75 ips (inches per second). Speed selection is determined by both a series of links and RC timing constants.

The illustration on the following page (Figure 2-2) shows the locations of the timing components and links that must be altered to support operation at a different drive speed. Refer to the following tables for component values and link positions.

TABLE 2-1
TAPE SPEED COMPONENT VALUES

TAPE SPEED (inches/second)	CAPACITORS (uF)			RESISTORS			CRYSTAL FREQUENCY
	C41	C35	C36	R47	R39	R38	
12.5	Ø.1	Ø.ØØ33	Ø.ØØ33	41.2k	37.4k	28.Øk	4.2 MHz
15	Ø.1	Ø.ØØ33	Ø.ØØ22	3Ø.9k	3Ø.9k	34.Øk	4.2 MHz
25	Ø.ØØ47	Ø.ØØ22	Ø.Ø1	35.7k	28.Øk	34.Øk	4.2 MHz
37.5	Ø.ØØ22	Ø.Ø1	Ø.Ø1	49.9k	41.2k	28.Øk	4.2 MHz
45	Ø.ØØ22	Ø.Ø1	Ø.Ø1	41.2k	35.7k	23.2k	5.Ø4 MHz
75	Ø.ØØ22	Ø.Ø1	Ø.Ø1	25.5k	2Ø.Øk	13.3k	4.2 MHz

Note: Refer to parts list in Section 5 for complete component descriptions.

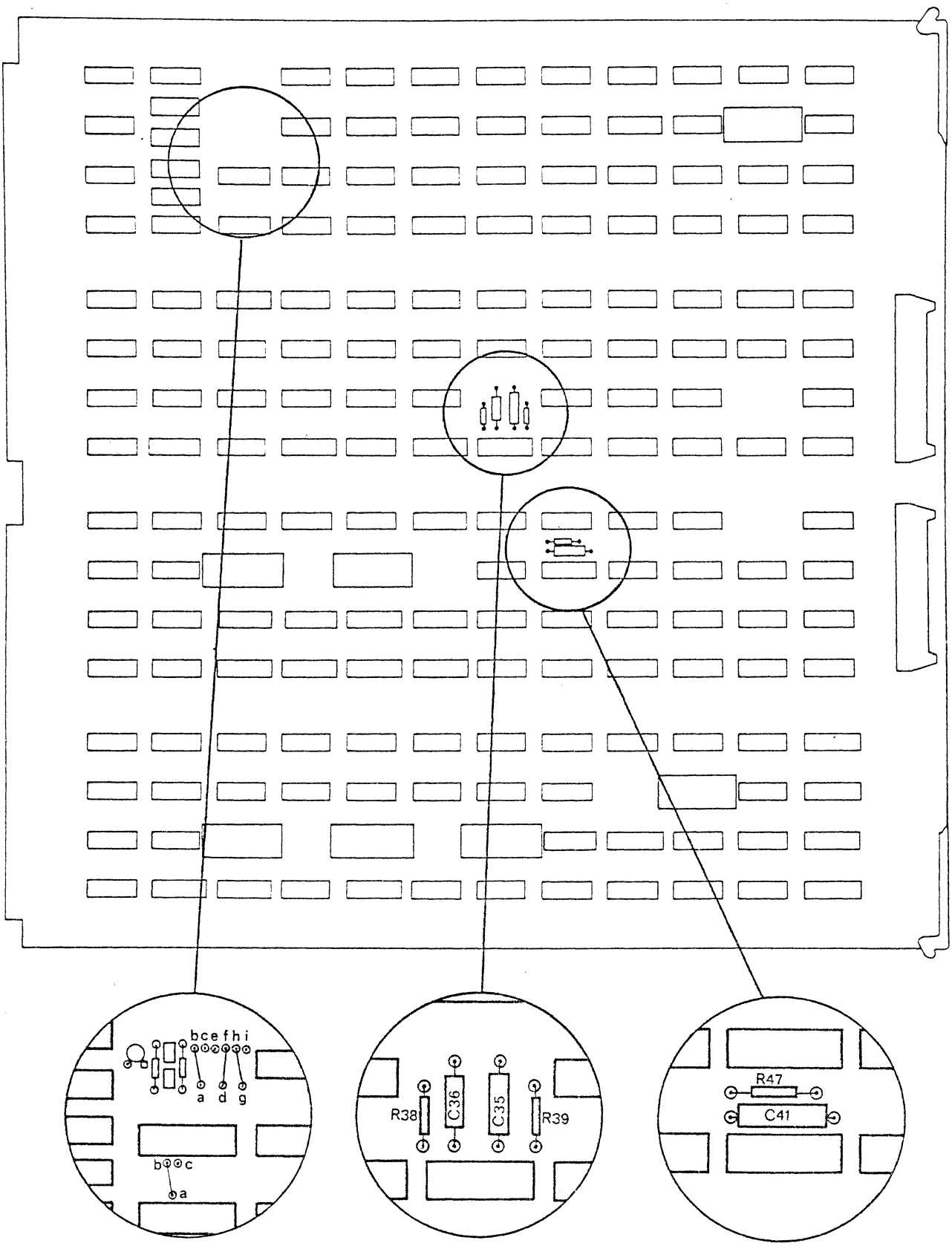


FIGURE 2-2

SPEED SELECTION LINK AND COMPONENT LOCATIONS

TABLE 2-2A

TAPE SPEED LINKS

TAPE SPEED	LINKS	LOCATION
12.5	a-c d-e g-i	C2
15	a-b d-e g-i	
25	a-b d-f g-h	
37.5	a-c d-e g-h	
45	a-c d-e g-h	
75	Irrelevant (see Table 2-2B)	

TABLE 2-2B

75 IPS TAPE SPEED LINK

TAPE SPEED	LINKS	LOCATION
75	a-c	C3
All Others	b-c	

2.5.2.2 Device Code Selection

Two device codes are available for the controller: device codes 22_8 and 62_8. Unless otherwise specified, the controller will be configured to respond to device code 22_8. To change to device code 62_8, two links must be changed. The diagram on the following page (Figure 2-3) and the ensuing table define the device code link locations and configurations for the two available device codes.

TABLE 2-3
DEVICE SELECT LINKS

DEVICE CODE	LINKS	LOCATIONS
22_8	a-b	A14 B5
62_8	a-c	A14 B5

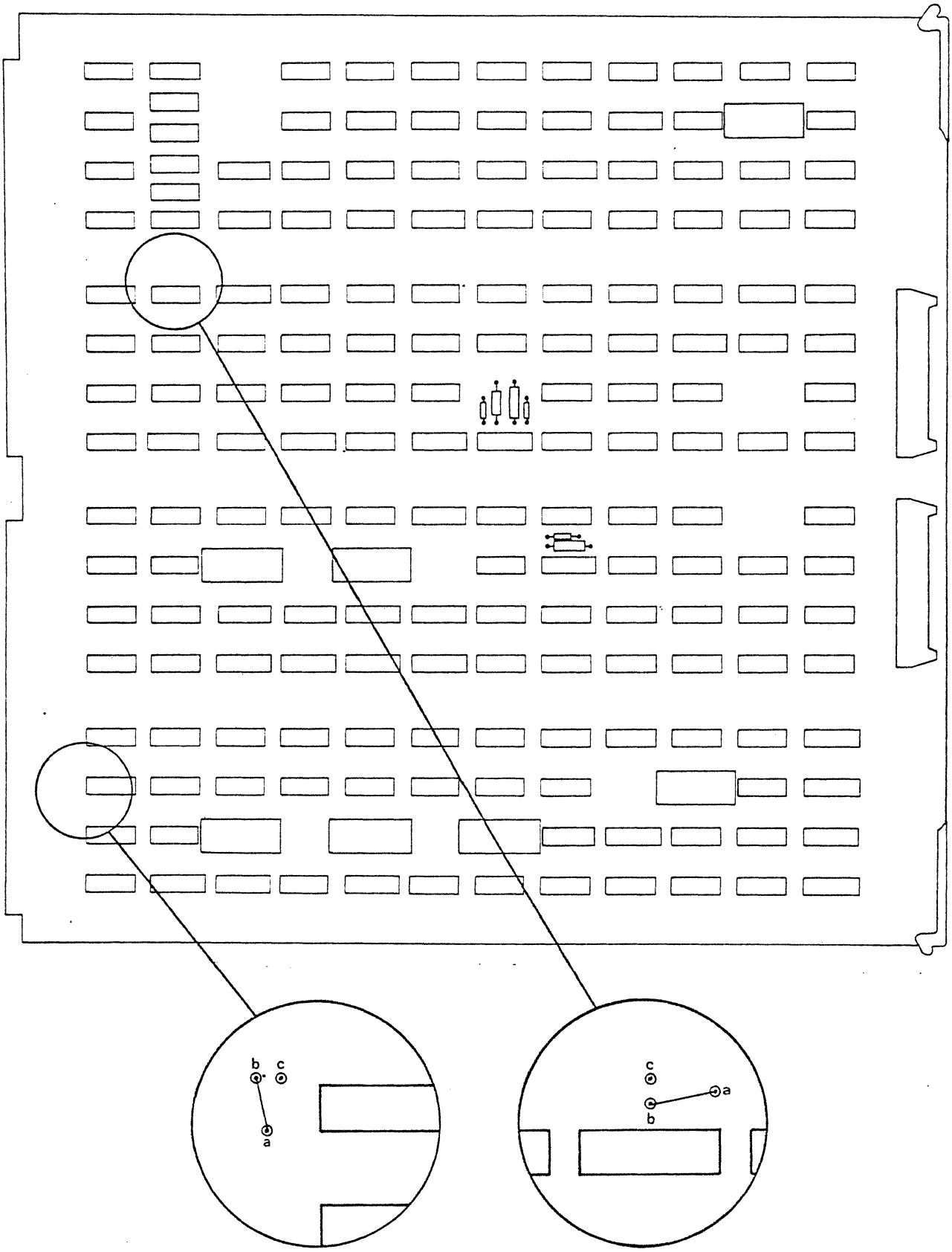


FIGURE 2-3

DEVICE CODE LINK LOCATIONS

2.5.2.3 Mask Bit Selection

The standard mask bit for the 3120 Controller is 1Ø. Any other mask bit can be selected by changing the link at M1Ø from a-b to a-c and then hard-wiring the desired mask bit from the location specified in Table 2-4 to the small unlabeled pad adjacent to pad c.

TABLE 2-4
MASK BIT ORIGINS

MASK BIT	SIGNAL NAME	IC ORIGIN
8	IDATA 8	E13, pin 11
9	IDATA 9	E13, pin 3
11	IDATA 11	E13, pin 4
12	IDATA 12	F13, pin 11
13	IDATA 13	F13, pin 3

Note: Refer to schematic 96-0204214-1, sheet 18 for additional mask bit origins.

When wiring an alternate mask bit, use insulated 26 AWG solid wire. Solder one end of the wire directly to the appropriate IC lead and route the wire along the top (component) side of the logic card, keeping the length as short as possible. Ensure that the lead protruding from the bottom of the logic card is clipped short. Refer to the diagram on the following page (Figure 2-4) for link and IC locations.

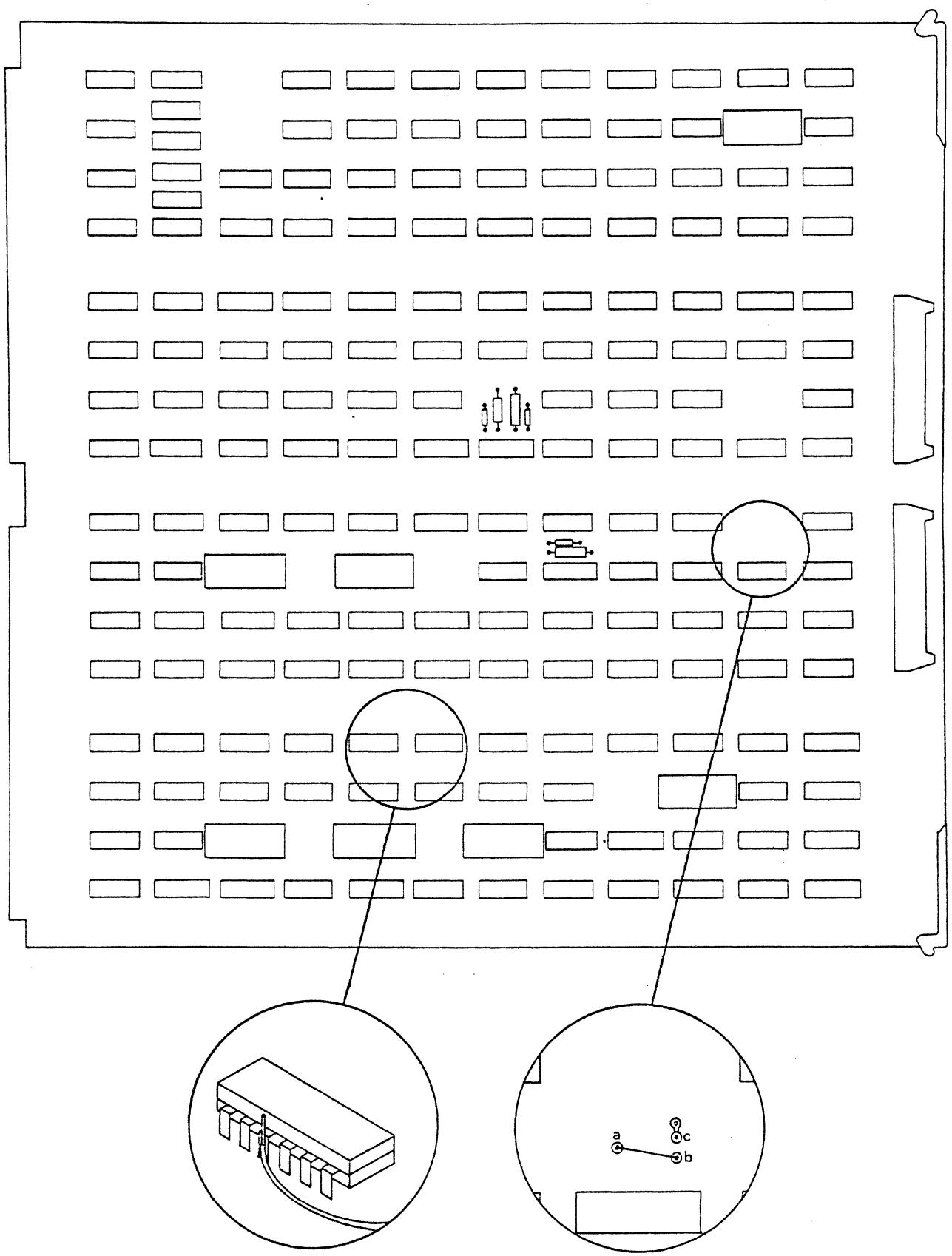


FIGURE 2-4

MASK BIT LINK LOCATION

2.5.2.4 Track Format Selection

The track format links identify the drive (or drives) as either 7-track or 9-track. Referring to Figure 2-5 and the following table, four individual link positions are available. Installing a link in any position identifies the corresponding drive as a 9-track unit while omitting (or removing) a link identifies the corresponding drive as 7-track. Unless otherwise specified, a single link is installed at a-b, identifying drive (unit) Ø as 9-track and all other drives (if any) as 7-track.

TABLE 2-5
TRACK FORMAT SELECTION LINKS

9 TRACK SELECT	*LINK	LOCATION
Unit Ø	a-b	K14
Unit 1	c-d	
Unit 2	e-f	
Unit 3	g-h	

*Omit links for 7-track drives.

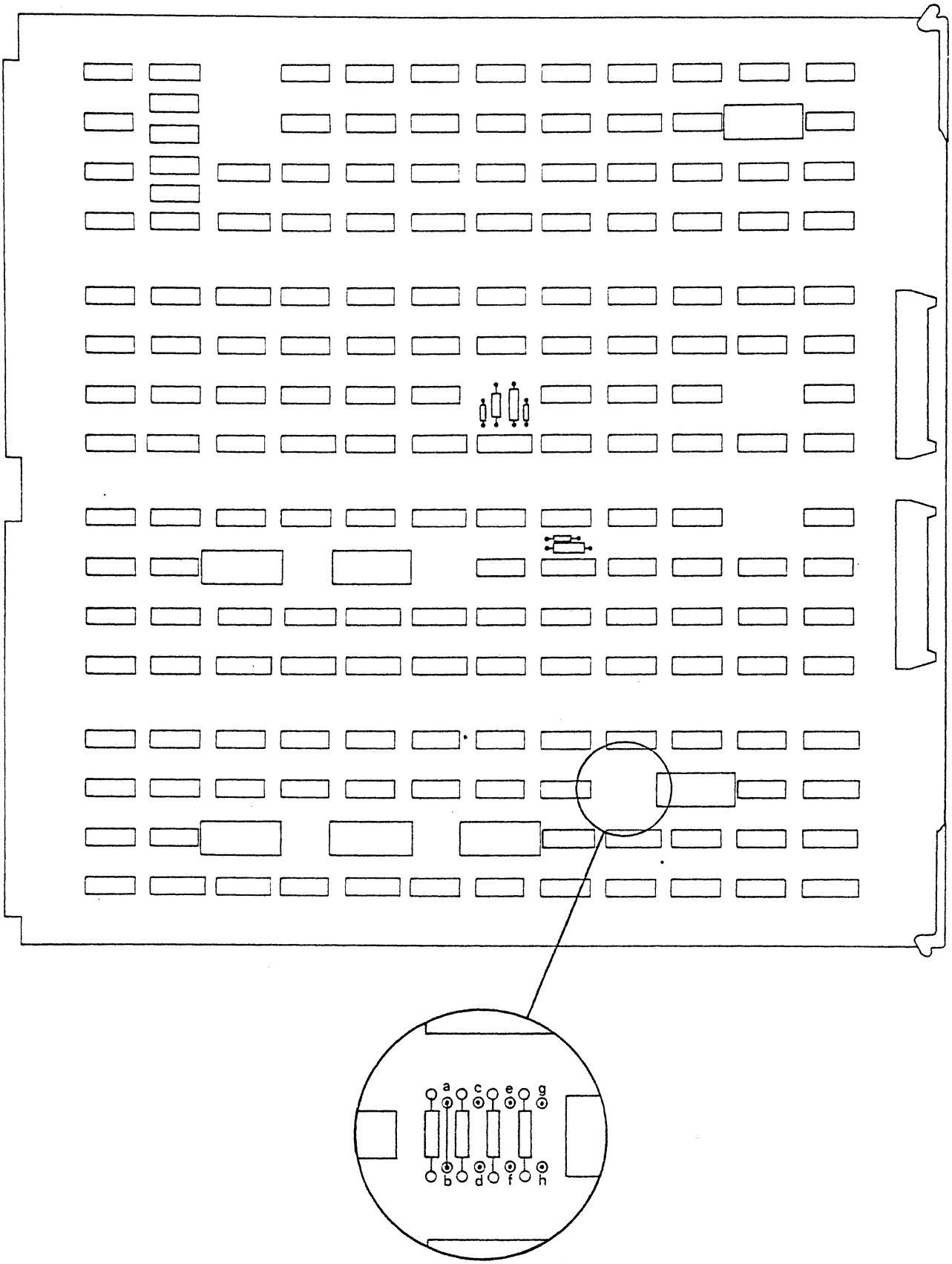


FIGURE 2-5

TRACK FORMAT LINK LOCATION

2.5.2.5 Word Transfer Length

The maximum number of words that can be transferred within a single record is fixed at either 4K or 32K. The number of words transferred is determined by the link at location D13. Unless otherwise specified, the link is installed between pads a-b, fixing the maximum number of words transferred at 32K. The alternate 4K position (a-c) can be used as an additional safeguard when it is possible to encounter large records on systems with limited core. Since the number of words transferred is normally specified by the program, changing this link is usually unnecessary and also limits the length of all records at 4K.

2.5.2.6 Special Links

The controller includes three sets of links which are reserved for special applications. As shown on the following illustration, these links are located at C6, K3 and M12. Unless required, the links will be installed as noted in the following table.

TABLE 2-6
SPECIAL LINKS

LINK	LOCATION
a-c	C6
a-b	K3
a-b	M12

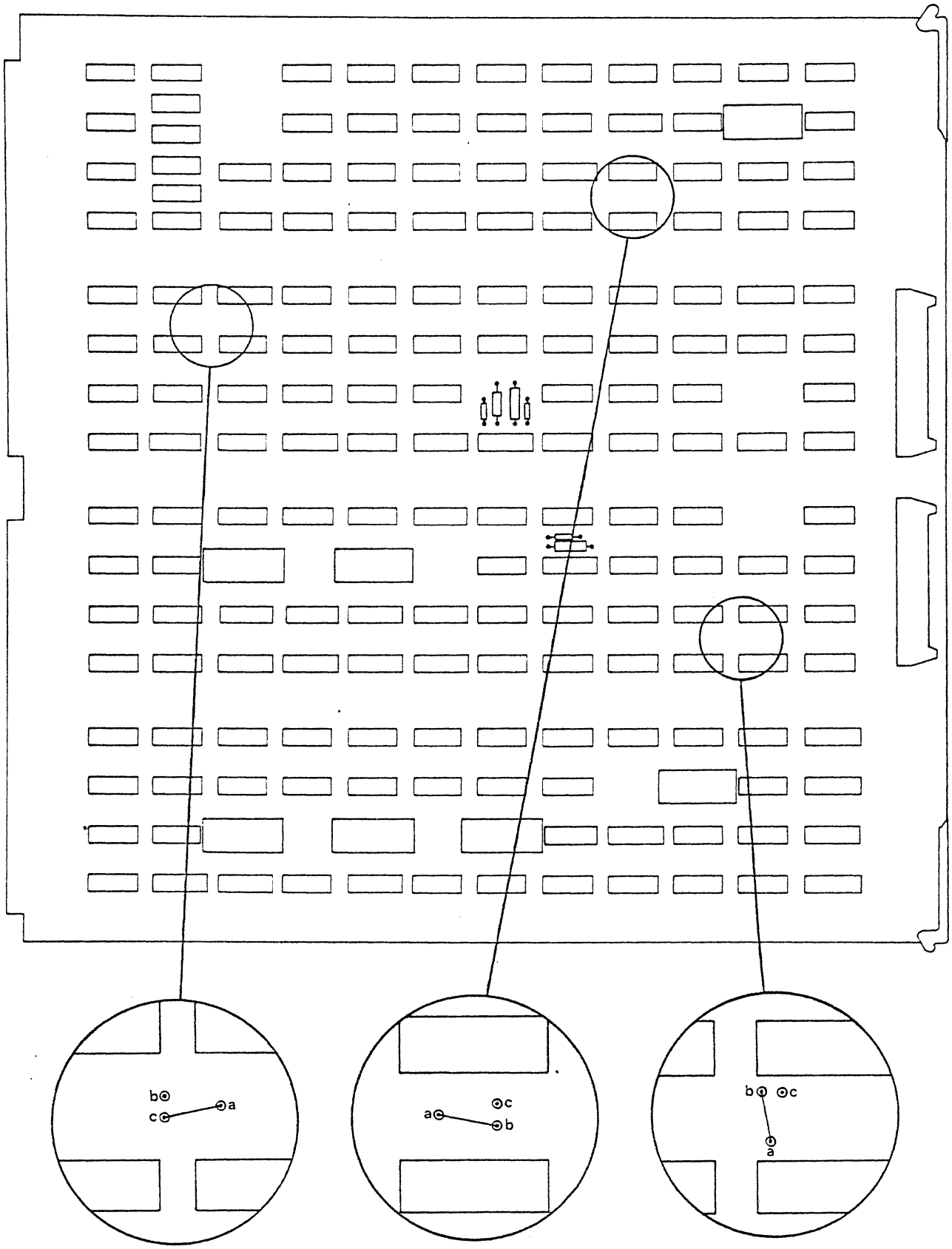


FIGURE 2-6

SPECIAL LINK LOCATIONS

2.5.2.7 3180/20 Option Links

When the 3120 Controller is used in conjunction with the 3180 PE Controller, the drive configuration must be identified on the 3120 Controller logic card. Referring to the following illustration (Figure 2-7), the logic card incorporates a number of wire-wrap pins at location M8. Pins a, b and c are cross-connected to pins 1, 2, 3 or 4 to match the drive unit number with its corresponding configuration according to the following table.

TABLE 2-7
3180/20 CONFIGURATION LINKS

DRIVE NUMBER	DRIVE CONFIGURATION				LOCATION
	PE ONLY	*PE/NRZI	**PE/NRZI	NRZI	
DRIVE Ø	4-b	4-c	4-a	No Connect	M8
DRIVE 1	2-b	2-c	2-a	No Connect	
DRIVE 2	1-b	1-c	1-a	No Connect	
DRIVE 3	3-b	3-c	3-a	No Connect	

*Program Selectable
**Manually (switch) Selectable

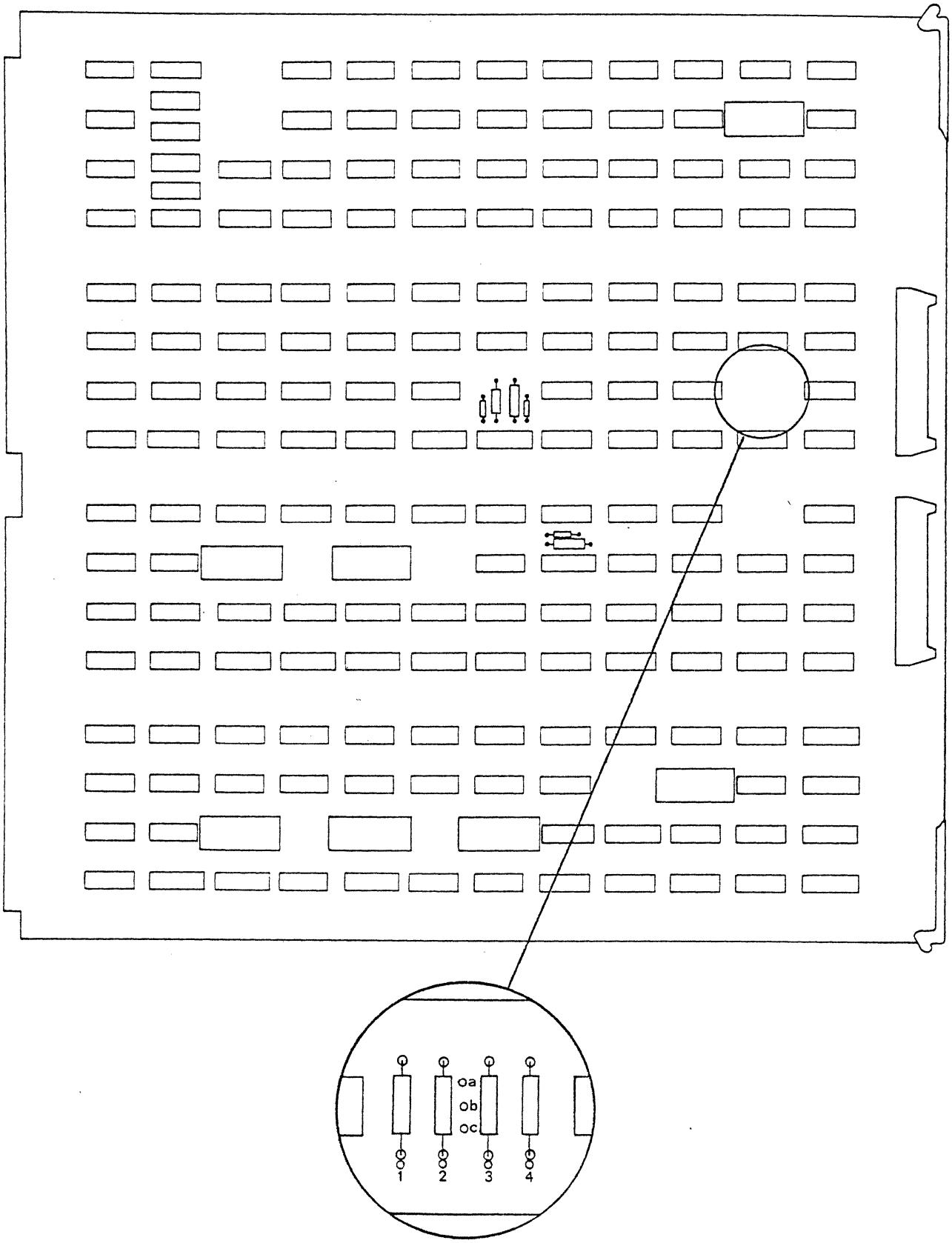


FIGURE 2-7

3180/20 OPTION LINK LOCATION

2.5.3 Adapter Assembly

The adapter assembly supplied is mounted either within or external to the tape drive depending on the drive manufacturer and model. To facilitate mounting, four stand-offs are included on the rear of the adapter pc board. Refer to the corresponding appendix at the conclusion of this manual for drive interface cabling requirements to determine possible mounting locations. Use the supplied adapter mounting hardware to secure the adapter assembly in place.

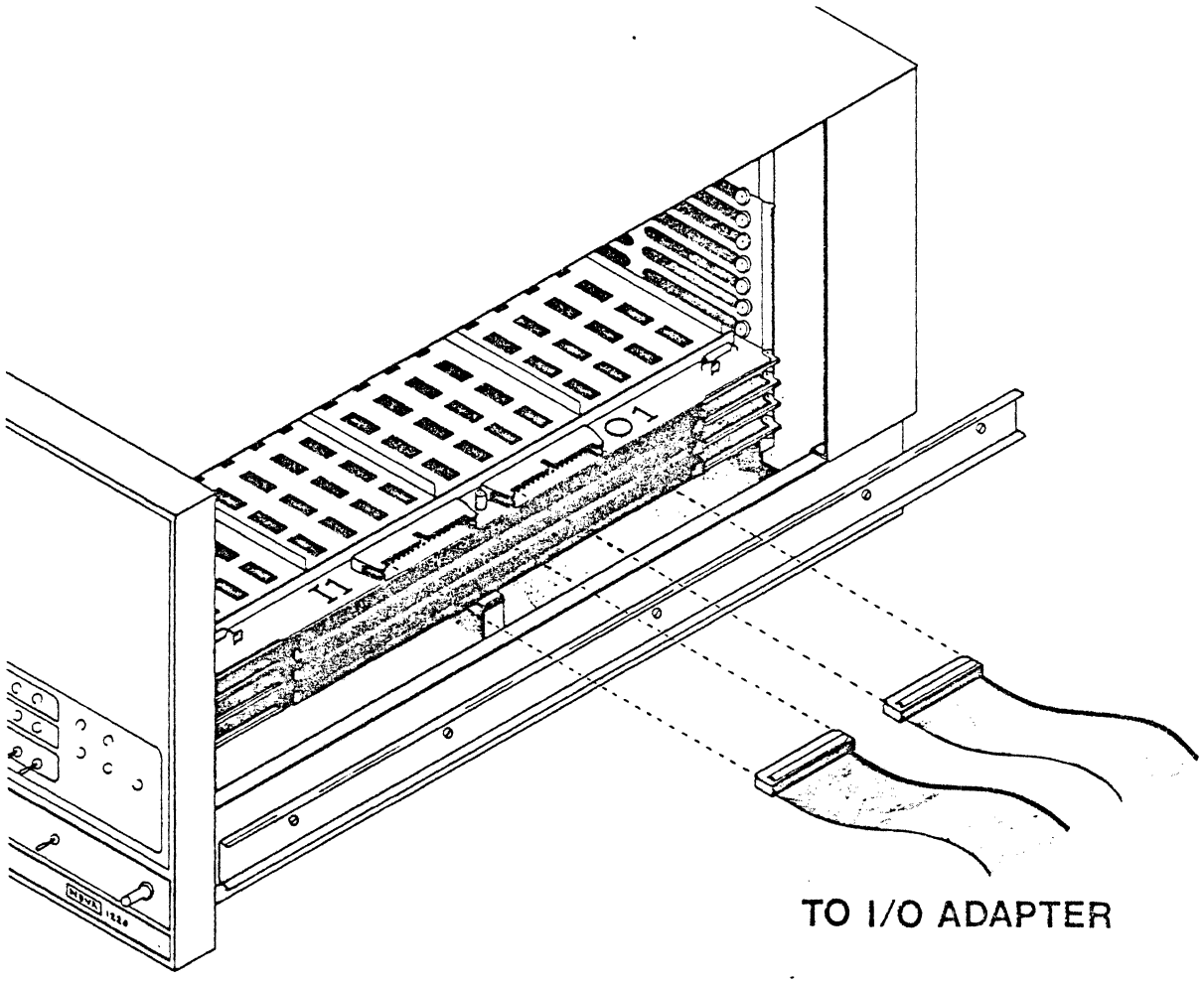
2.5.4 Logic Card-to-Adapter Interface

After mounting the adapter assembly, the logic card-to-adapter interface cables are installed. The logic card is fitted with two edge-connectors designated I1 and O1. Generally, the mating connectors at each end of the interface cables are labeled at the factory with their corresponding interface connector. Locate the cable end marked "controller O1" and insert it into edge-connector O1 on the logic card. Orient the cable from the mating connector to exit from the under-side of the edge-connector as shown in the detail of Figure 2-8.

NOTE

The protective fiberglass insulator, mounted on the component side of the logic card, has been intentionally omitted from the illustration to increase clarity.

If the interface cable mating connectors are not marked, either cable can be used (the cables are identical). Insert the cable end, which arranges the reference red stripe to appear on the right-hand edge of the cable when properly installed, into connector O1 on the logic card. Mark the mating connector at the remaining end of this cable so that it can be readily identified. Similarly, insert the appropriate end of the remaining interface cable into edge-connector I1, again orienting the cable from the mating connector to exit from the under-side of the edge-connector and with the reference red stripe appearing on the right-hand edge of the cable.



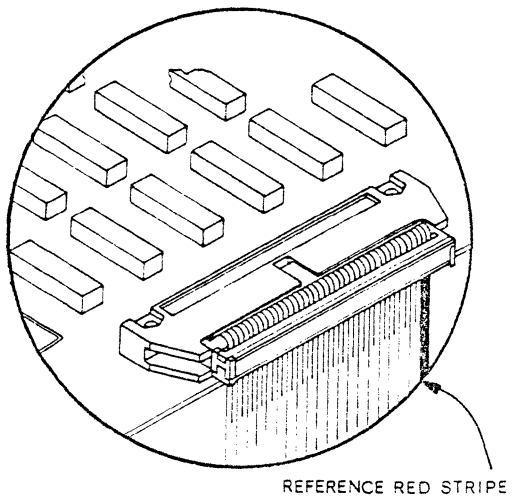


FIGURE 2-8
LOGIC CARD INTERFACE

CAUTION

Never remove a cable from its connector by pulling on the cable directly. Use the supplied 3M No. 3438 extractor tool or insert a small screwdriver into the recessed slot on the top of the connector, twisting gently to separate.

After installing the cables, fold at 90° and route along the right side of the computer chassis to the rear of the computer as shown in Figure 2-9. Apply a small amount of adhesive to the inside of the folds to prevent the cables from protruding outwards and secure the cables to the rear of the chassis to ensure clearance between the computer and the right-side of the enclosure. To secure the cables, use a strain relief (shown), strong tape or Velcro®.

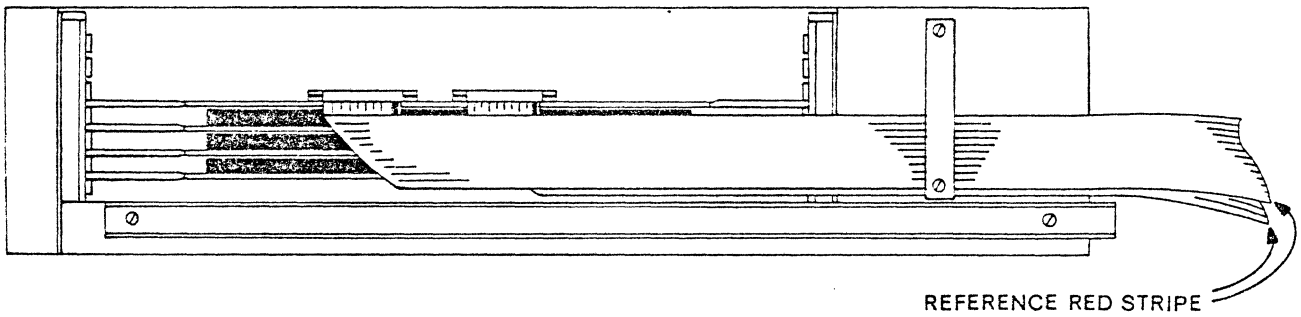


FIGURE 2-9
CABLE ROUTING

After securing the cables in place, the computer should be installed in the enclosure or slid into position, draping the cables down into the bottom of the enclosure. Referring to Figure 2-10, insert the cable from connector 01 on the logic card (labeled "adapter 01" or previously marked) into connector

O1 on the adapter assembly, arranging the cable as shown. Similarly, insert the cable from connector I1 on the logic card (marked "adapter I1" or unlabeled) into connector I1 on the adapter assembly. Dress any excess cable slack within the enclosure, allowing sufficient length to permit the computer to be slid out of the enclosure.

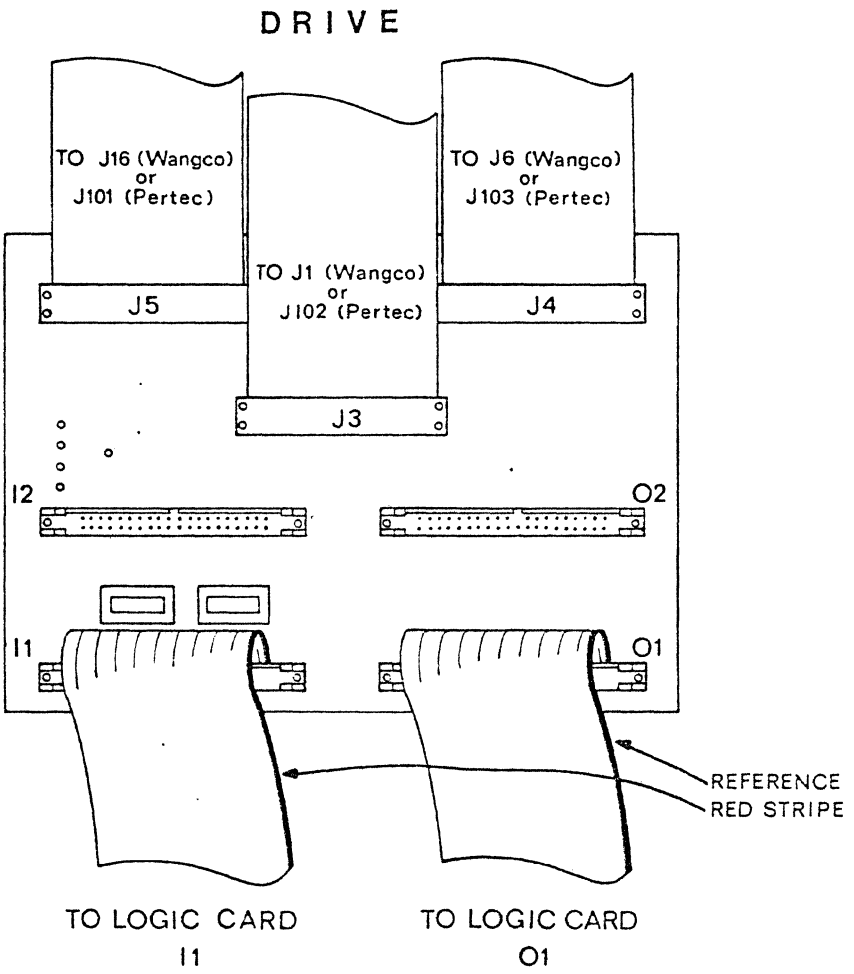


FIGURE 2-10
I/O ADAPTER ASSEMBLY INTERFACE

2.5.5 Adapter - Drive Interface

The adapter assembly supplied incorporates three drive interface cables which are terminated with the proper mating connectors to interface directly with the type of drive specified. Refer to the appropriate appendix at the conclusion of this manual for detailed instructions on the type of drive to be interfaced.

2.6 MULTIPLE-DRIVE INTERFACE

Up to four tape drives can be interfaced to the 3120 Controller using a "daisy-chain" technique. The termination networks (or termination resistors) in all but the last drive must be removed (see corresponding appendix). To connect multiple drives, interface the controller to the adapter assembly of the first drive as described in subsection 2.5.4 Referring to Figure 2-11, insert one end of a daisy-chain (or controller-to-adapter) interface cable into connector I2 on the first drive's adapter assembly. Insert the remaining end of this cable into connector I1 on the second drive's adapter assembly. Similarly, connect one end of the other daisy-chain cable to connector O2 on the first drive's adapter assembly and the remaining end to connector O1 on the second drive's adapter assembly. Continued this procedure for each drive in the system.

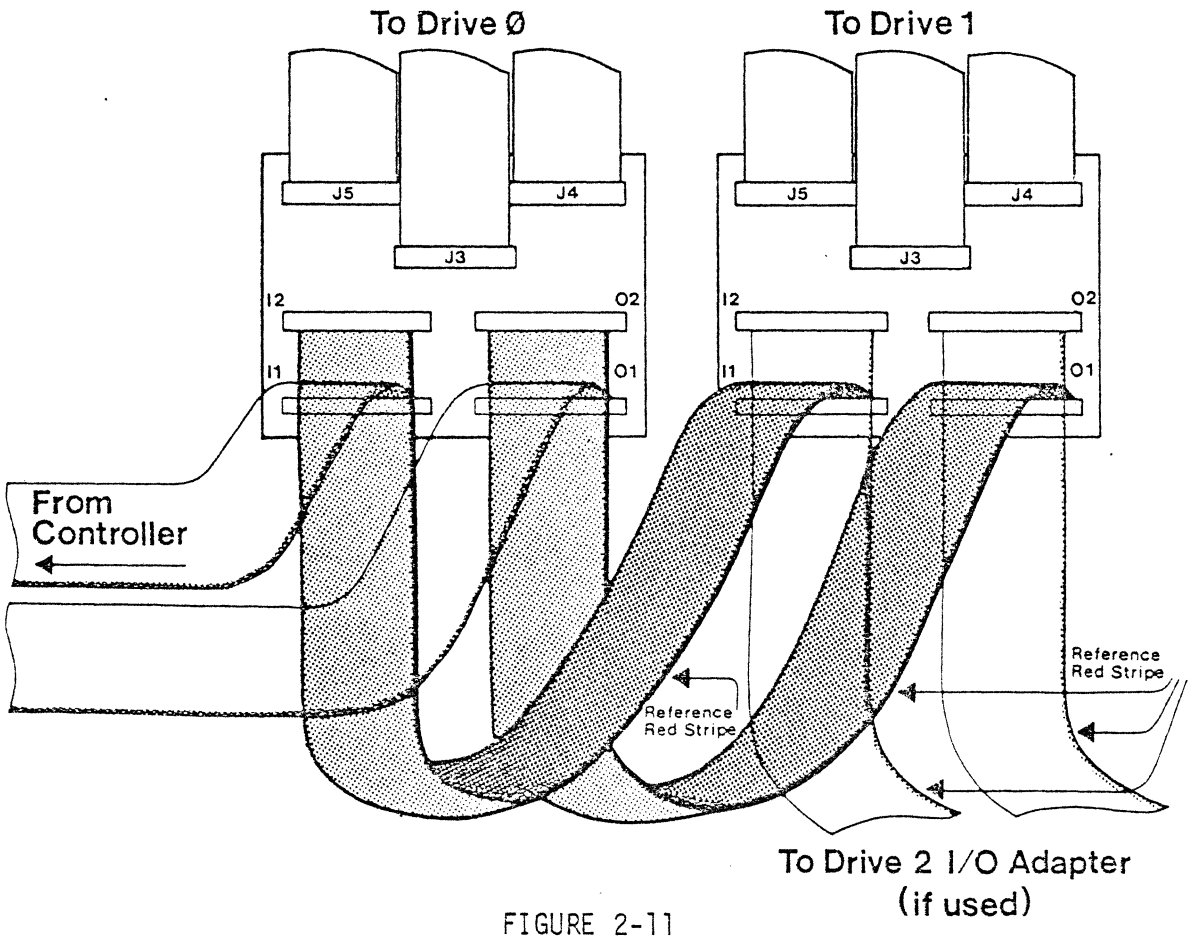


FIGURE 2-11
MULTIPLE-DRIVE INTERFACE

After interfacing is complete, ensure that the drive select jumper on each adapter assembly is set to the correct drive number. Referring to the following illustration (Figure 2-12), the drive select cross-connect matrix is located at the center of the left-hand edge of the adapter card. Terminals 0, 1, 2 and 3 correspond to the drive unit number. The drive is, in turn, selected by inserting a wire strap between the desired unit number and terminal "S".

NOTE

Drive numbers may be assigned in random order. All drives within the same system must, however, be assigned a unique drive number.

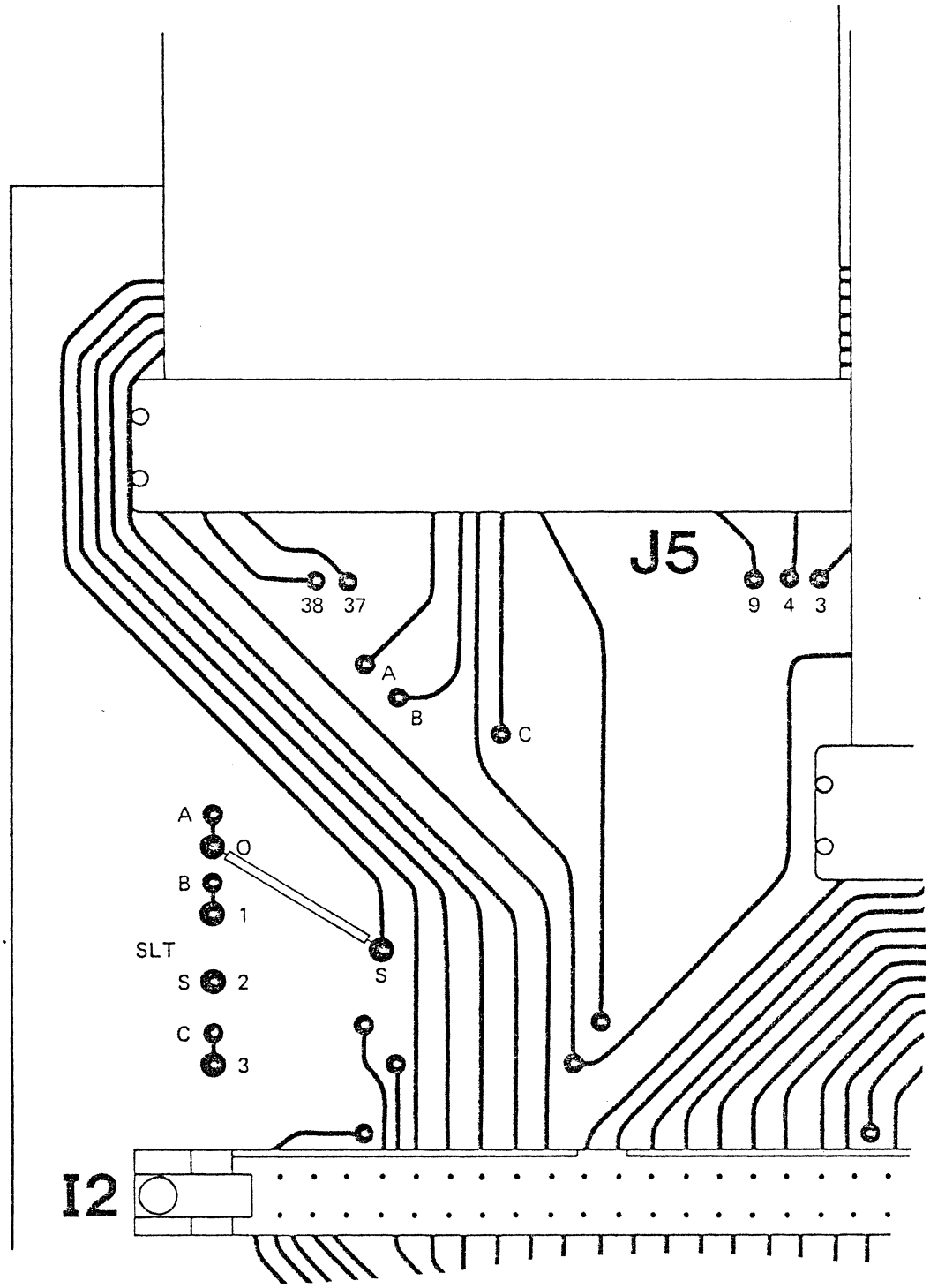


FIGURE 2-12
DRIVE SELECTION STRAPPING

2.7 3180/20 OPTION INTERFACE

The 3180/20 Option consists of a 3120 NRZI Controller and a 3180 PE Controller interfaced to the drive(s) on a common bus. A special controller-to-adapter cable interface is supplied which connects both controllers to a single I/O adapter assembly.

Insert the 3120 logic card into the selected I/O slot. The controller should occupy the lower of the two selected slots. Prior to installing the 3180 Controller, refer to the following table and remove the 220/330 ohm termination resistor pairs at the inputs to the deskewing buffers (READ DATA) and at the status inputs to the transport status command decoder logic.

NOTE

Ensure that the data channel and interrupt priorities are maintained on the CPU back panel if a vacant slot or slots exist between the two controllers (see Section 2.5.1).

Referring to the illustration on page 2-27 (Figure 2-13), connect the cable assembly as shown. The individual cable mating connectors are labled with their corresponding pc card connectors.

On the back panel of the CPU, install a wire-wrap jumper from pin B52 of the I/O slot occupied by the 3120 Controller to pin A61 of the I/O slot occupied by the 3180 Controller.

3180 PC CARD

RESISTOR REMOVAL

RESISTOR PAIR	SIGNAL NOMENCLATURE	PC CARD COORDINATES
R19,R20	READ DATA P	Z5
R21,R22	READ DATA Ø	R5
R23,R24	READ DATA 1	R15
R25,R26	READ DATA 2	R15
R27,R28	READ DATA 3	V11
R39,R40	READ DATA 4	N7
R31,R32	READ DATA 5	Z3
R33,R34	READ DATA 6	U3
R35,R36	READ DATA 7	Z4
R45,R46	REWIND STATUS	P15
R47,R48	FILE PROTECT STATUS	P15
R49,*R50	BOT STATUS	M13,M15
R51,R52	READY STATUS	P15
R53,R54	EOT STATUS	P15

*Resistor R50 on the schematic has been incorrectly labeled R5 on the PC card silkscreen.

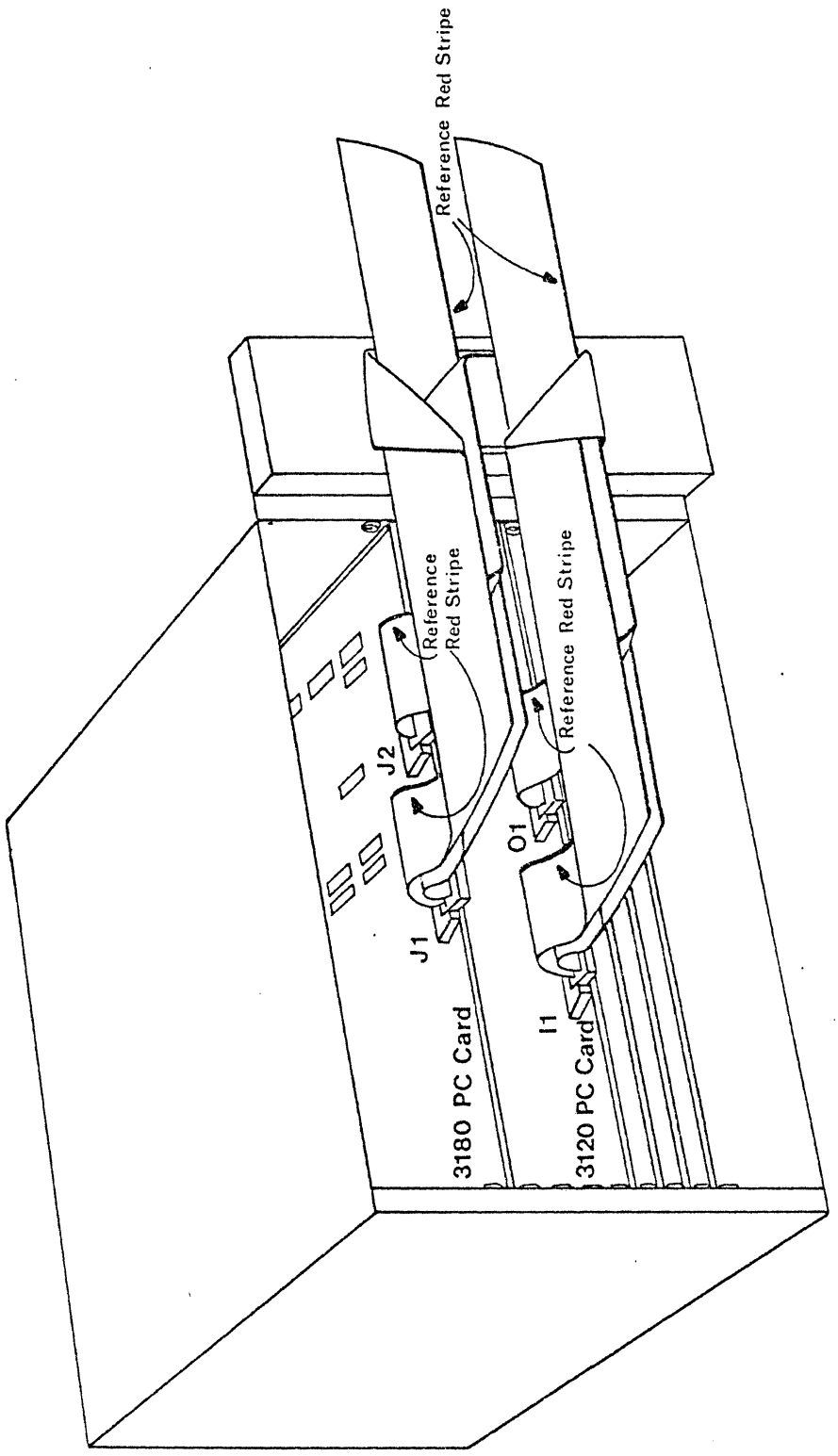


FIGURE 2-13
3180/20 OPTION INTERFACE

2.8 OPERATION

Following installation, operation of the 3120 Controller can be verified using the 3120/3180 Mag Tape Reliability program. Apply power to both the drive and CPU and, following the instructions in the corresponding manual, load and run the reliability program. This program verifies proper operation of both the controller and tape drive and should be allowed to run until 10^8 characters have been transferred (typically 2 to 6 hours depending on tape speed).

SECTION 3
PROGRAMMING CONVENTIONS

3.1 INTRODUCTION

This section describes the NRZI (Non-Return-Zero-Inverted) recording technique, tape format and programming conventions for the 3120 Tape Controller.

3.2 NRZI RECORDING

With the NRZI technique, information is recorded by altering the direction of magnetization (flux) at the boundary of the bit cell. A change in the direction of flux from a negative saturation level to a positive saturation level is defined as a "1" while a "0" is represented by no change in the flux direction (saturation level remains negative). The following illustration shows the flux transitions for the bit sequence Ø11ØØØ1.

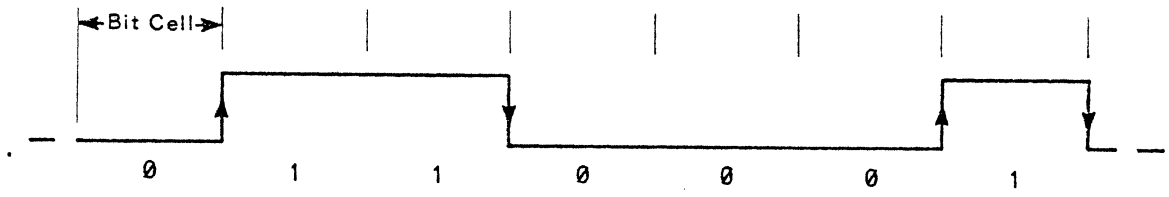


FIGURE 3-1
BIT CELL FLUX TRANSITION

3.3 TAPE ORGANIZATION

The controller supports operation in either the IBM compatible 7-track format or the ANSI compatible 9-track format. Data on the tape is grouped into records and files. Each record is separated by an erased gap (inter-record gap) while groups of records are partitioned into files through the use of file marks. At the conclusion of each data record, either one or two check

characters are recorded and the inter-record gap (IRG) is inserted.

3.3.1 Record Format

The record formats for both the 7- and 9-track formats are shown in the following illustration (Figure 3-2). The initial record on the tape (first record following the beginning-of-tape reflective marker) is preceded by an initial erased gap of three inches. Following the last character of each record, the check character (or characters) is written and an IRG is erased on the tape. Referring to the illustrations, only a longitudinal redundancy check (LRC) character is written in the 7-track format while both an LRC and a CRC (Cyclic Redundancy Check) character are written in the 9-track format. The inter-record gap is nominally 0.6 inches in the 9-track format and 0.75 inches in the 7-track format.

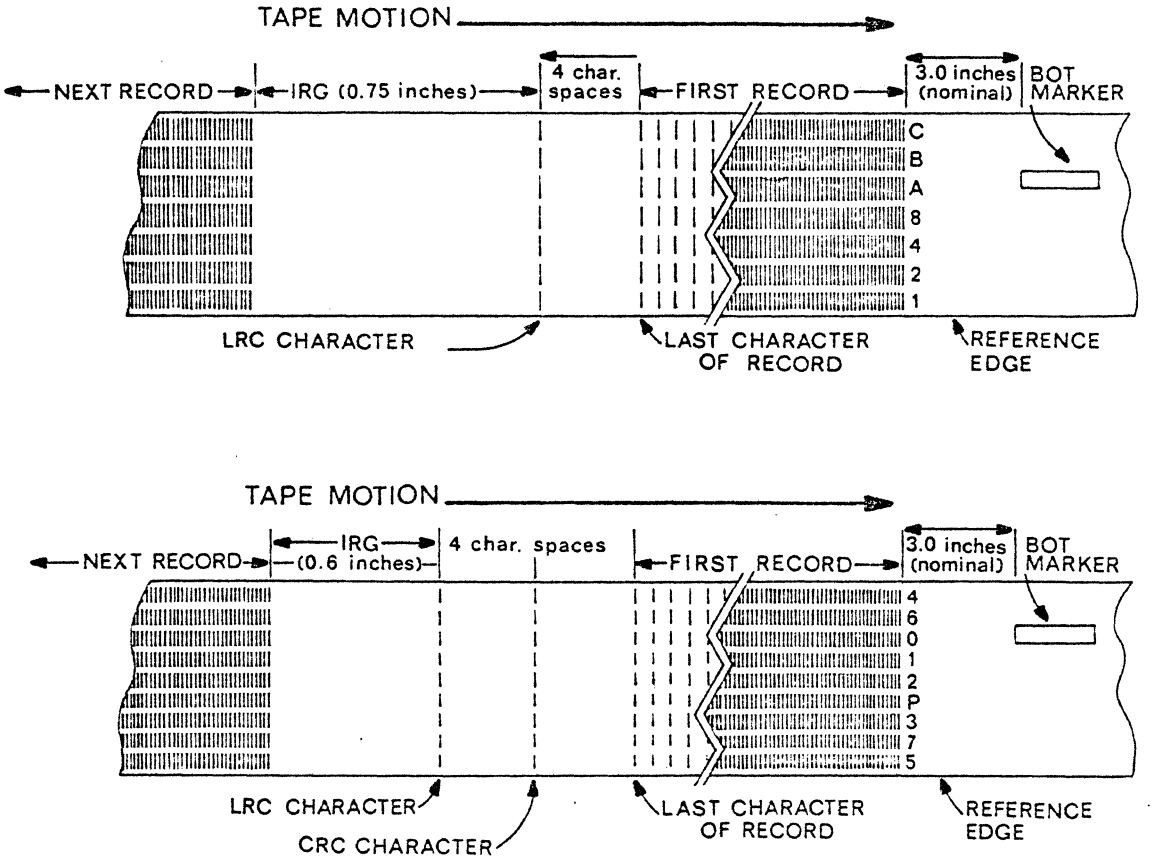


FIGURE 3-2
RECORD FORMATS

3.3.2 File Format

A group of records is separated by an end-of-file (EOF) mark, a unique one character record. As shown in Figure 3-3, the file mark differs for the 7-track and 9-track formats. In the 7-track format, a "1" bit is written in channels 1, 2, 4 and 8 (only) while in the 9-track format, a "1" bit is written only in channels 3, 6 and 7. The EOF mark is, in turn, followed by an LRC character. In the 7-track format, the EOF mark is preceded by an erase gap of 3.9 inches (nominally) and followed by the LRC character (separated by four character spaces). In the 9-track format, the erase gap between the LRC of the last record and the EOF mark is 3.75 inches (nominally) with the end-of-file LRC character separated by eight character spaces. A CRC is not written for the end-of-file record in the 9-track format.

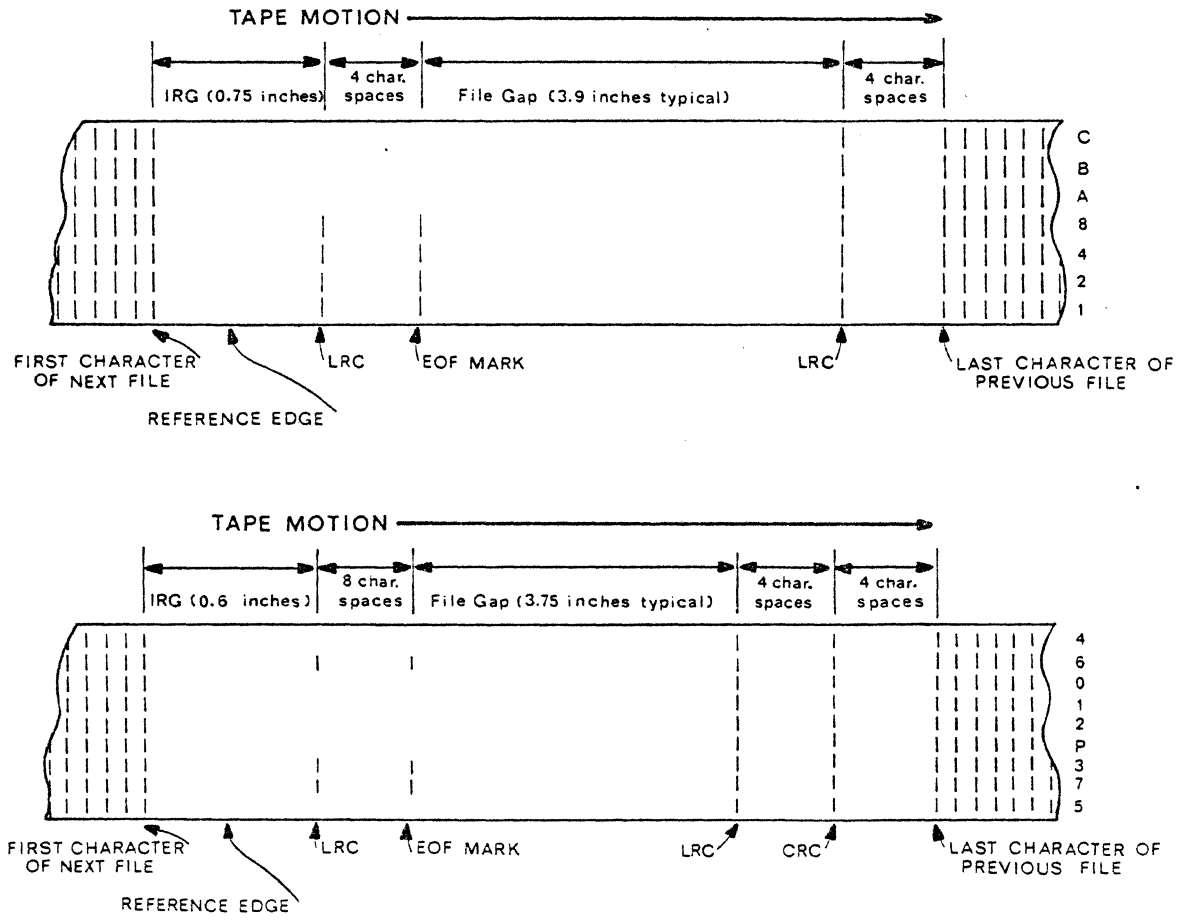
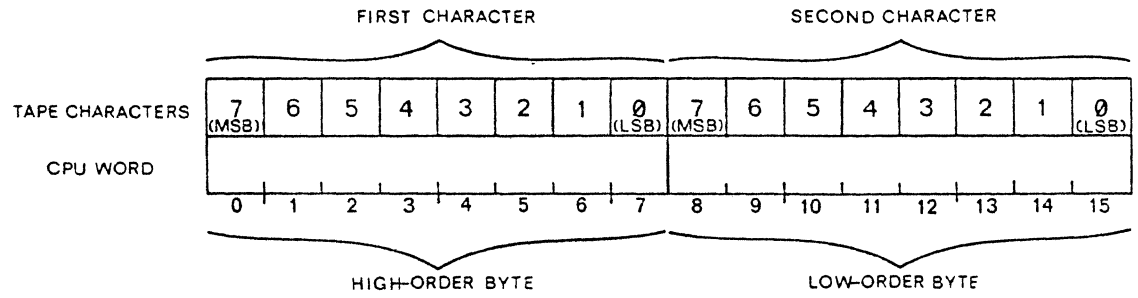


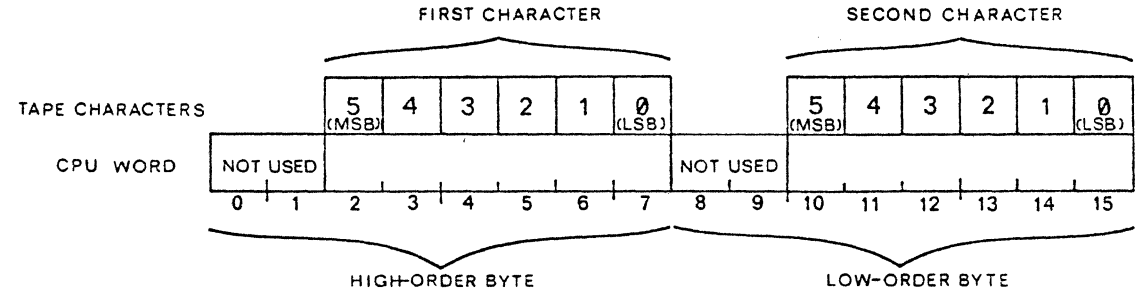
FIGURE 3-3
FILE MARK FORMATS

3.3.3 Word Format

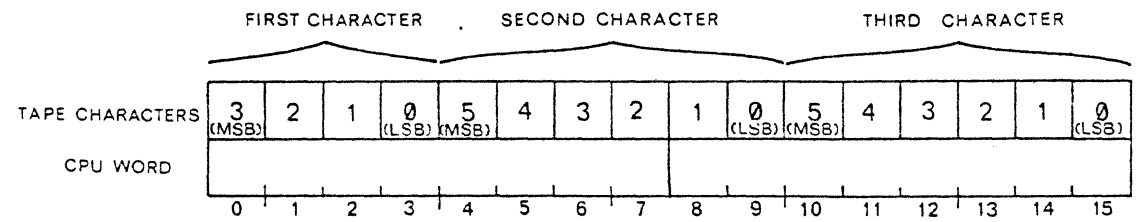
9-track characters consist of eight data bits and a parity bit. The controller assembles the data bits of two tape characters into a sixteen bit word as shown.


FIRST CHARACTER
SECOND CHARACTER
TAPE CHARACTERS
7 (MSB) 6 5 4 3 2 1 0 (LSB)
7 (MSB) 6 5 4 3 2 1 0 (LSB)
CPU WORD
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
HIGH-ORDER BYTE
LOW-ORDER BYTE

7-track characters consist of six data bits and a parity bit. Characters can be assembled into a sixteen bit word in either a two- or three-character mode. In the two-character mode, bits 0 and 1 of the high-order byte and bits 8 and 9 of the low-order byte are not used.


FIRST CHARACTER
SECOND CHARACTER
TAPE CHARACTERS
5 (MSB) 4 3 2 1 0 (LSB)
5 (MSB) 4 3 2 1 0 (LSB)
CPU WORD
NOT USED
NOT USED
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
HIGH-ORDER BYTE
LOW-ORDER BYTE

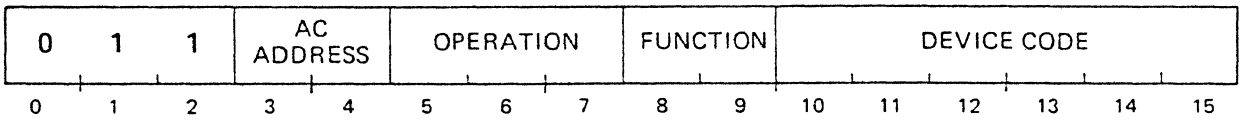
In the three-character mode, three tape characters are assembled into a single sixteen bit word. The first two bits of the first character are not used.


FIRST CHARACTER
SECOND CHARACTER
THIRD CHARACTER
TAPE CHARACTERS
3 (MSB) 2 1 0 (LSB)
5 (MSB) 4 3 2 1 0 (LSB)
5 (MSB) 4 3 2 1 0 (LSB)
CPU WORD
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

3.4 PROGRAMMING

All controller operations are under program control. The controller uses the CPU's data (DMA) channel to transfer information. The program must specify the operation to be performed, a starting memory address location for the data transferred and the number of words to be transferred.

The controller follows the CPU's conventions in the use of the Busy and Done flags, and the data channel and interrupt logic. The CPU I/O instruction words exhibit the following format:



Bits 0, 1 and 2 (Ø11) define the instruction as an I/O operation.

Bits 3 and 4 select one of the CPU's four accumulators as the source or destination of the control or status word transferred. Certain I/O instructions do not require an accumulator, causing bits 3 and 4 to be ignored.

Bits 5, 6 and 7 select the I/O operation to be performed, defining the direction of the transfer and the registers within the controller involved with the transfer. The interpretation of these bits is as follows:

OPERATION	BIT		
	5	6	7
DOA	Ø	1	Ø
DOB	1	Ø	Ø
DOC	1	1	Ø

OPERATION	BIT		
	5	6	7
DIA	Ø	Ø	1
DIB	Ø	1	1
DIC	1	Ø	1

Bits 8 and 9 select a function to be performed by the controller. A single instruction can specify both an operation and a function. The interpretation of these bits is as follows:

FUNCTION	BIT 8	BIT 9	MNEMONIC
NIO	Ø	Ø	None
NIOS	Ø	1	S
NIOC	1	Ø	C
NIOP	1	1	P

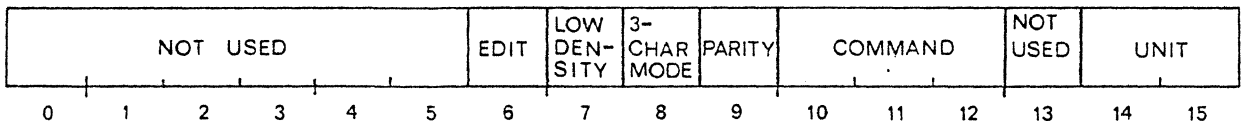
Bits 10 through 15 specify the octal device code. The 3120 Controller normally responds to device code 22_8, identified by the mnemonic MTA. (A simple adjustment can arrange the controller to respond to device code 62_8).

3.4.1 I/O Operations

The I/O operation is determined by the states of bits 5, 6 and 7 of the instruction word. The following operations transfer all control information to or from the controller.

Data Out A (DOA n, MTA)

The DOA instruction loads the contents of bits 6-15 from accumulator "n" (bits 3 and 4) into the controller's A (command) register.



Edit: The edit bit (bit 6) selects the optional edit mode available on certain drives. If the edit bit is set ("1"), the edit feature is enabled while if "0" the edit feature is disabled.

Low Density: The low-density bit (bit 7) is used with 7-track, remotely (CPU) selectable, dual-density

drives to select the desired recording density. If set ("1"), low density (556 cpi) recording is selected while if "0", high-density (800 cpi) recording is selected. When a manually-selectable, dual-density drive (or a fixed-density drive) is used, the density bit must correspond to the selected drive density for proper operation. The low-density bit is ignored with 9-track drives, automatically selecting high (800 cpi) density.

When the 3180/20 option is incorporated (for operating NRZI/PE combination drives with remote mode selection), the low-density bit is used to select either the 3120(NRZI) or 3180(PE) Controller. If the low-density bit is set ("1"), the 3180 controller is selected (at 1600 cpi) while if "0", the 3120 Controller is selected (at 800 cpi).

3-Char. Mode: The 3-char. mode bit (bit 8) is applicable only with 7-track drives and is used to select either the two- or three-character packing mode. If this bit is "1", the three-character mode is selected while if "0", the two-character mode is selected. This bit is ignored on 9-track drives.

Parity: The parity bit (bit 9) selects either even or odd parity across the character. A "0" selects odd parity while a "1" selects even parity. Odd parity is used predominately (bit 9=Ø) since an all-zero character with even parity is not recognized (appears as an erased gap).

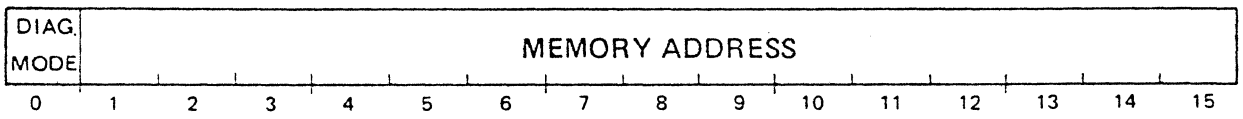
Operation: Bits 10-12 select the command to be executed by the next (or concurrent) Start (S) command as follows:

0 (000) - Read
1 (001) - Rewind
2 (010) - Off-Line
3 (011) - Space Forward
4 (100) - Space Reverse
5 (101) - Write
6 (110) - Write End-of-File
7 (111) - Erase

Drive: Bits 14 and 15 specify the addressed drive (0-3).

Data Out B (DOB n, MTA)

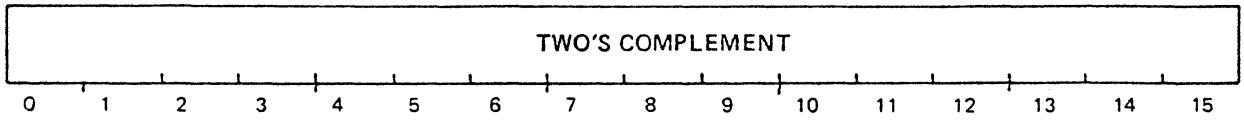
The DOB instruction loads the contents of the selected accumulator (n) into the controller's B (memory address) register.



Bits 1-15 of the accumulator word specify the memory location of the first data word to be transferred. The B register is subsequently incremented each time a word is transferred. Bit Ø, when set, selects the diagnostic mode, permitting the CRC character (9-track drives) to be transferred (read) into core. During a diagnostic read operation, one additional word is transferred. The CRC character is contained in the high-order byte (bits Ø-7) while the low-order byte is zero.

Data Out C (DOC n, MTA)

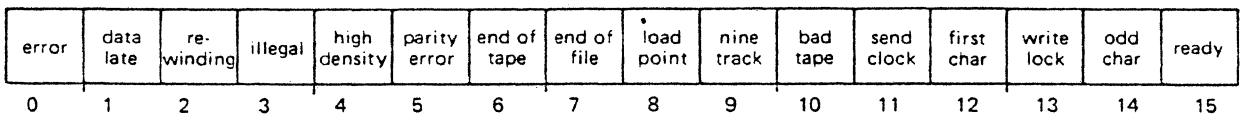
The DOC instruction loads bits Ø-15 of the selected accumulator (n) into the controller's C (word count) register.



When the controller is in the read or write mode, the register is loaded with the two's complement of the number of words to be transferred while when in the space forward or space reverse mode, the register is loaded with the two's complement of the number of records to be spaced over.

Data In A (DIA n, MTA)

The DIA instruction loads the specified accumulator with the contents of the controller's status register. The interpretation of the status register is as follows:



Bit 0: ERROR. An error has occurred as indicated by the setting of bits 1, 3, 5, 6, 7, 8, 10 or 14.

Bit 1: DATA LATE. The data channel did not respond to the controller's request for access within the required time period. The transfer will continue until either the end-of-record is reached or the word count is satisfied.

Bit 2: REWINDING. The addressed drive is currently rewinding.

Bit 3: ILLEGAL. This bit will be set if, when a start command is

issued, any of the following conditions exist:

1. The operation specified is "Write", "Erase" or "Write EOF" and the tape reel is not write-enabled (write-protect ring missing).

2. The operation specified is "Space Reverse" and the tape is at its load point (BOT) marker.

3. The addressed drive is not ready.

Setting "Illegal" prevents execution of further commands and causes the controller to set Done. Following an "Illegal" condition, a Clear (NIOC) command must be issued to clear the status register.

Bit 4: HIGH DENSITY. This bit reflects the selected recording density. A "1" indicates high (800 cpi) density while a "0" indicates low (556 cpi) density. With the 3180/20 option, a "1" indicates NRZI recording density (800 cpi) while a "0" indicates PE recording density (1600 cpi).

Bit 5: PARITY ERROR. This bit is set when the controller encounters a character or track with the "incorrect" parity.

Bit 6: END OF TAPE. This bit is set when the End-of-Tape (EOT) reflective marker is encountered.

Bit 7: END OF FILE. This bit is set whenever the controller writes, reads or spaces over an End-of-File (EOF) mark.

Bit 8: LOAD POINT. When set, this bit indicates that the tape is at the load point (BOT) marker.

Bit 9: NINE TRACK. This bit reflects the selected track format. A "1" indicates 9-track while a "0" indicates 7-track.

Bit 10: BAD TAPE. This bit, when set, indicates that during a read operation, data has been detected in the record gap (IRG) following the data record.

Bit 11: SEND CLOCK. A diagnostic bit which is set whenever the controller starts or stops the tape drive.

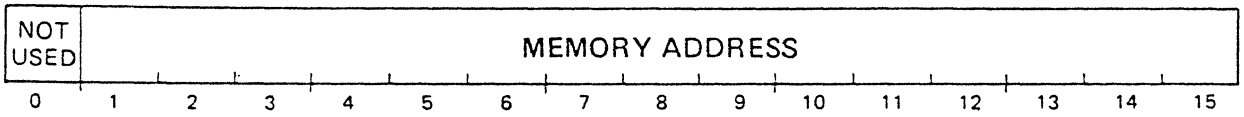
Bit 12: FIRST CHARACTER. A diagnostic bit set when the first character of a data record is read.

Bit 13: WRITE LOCK. When set, this bit indicates that the write enable ring is not in place on the source tape reel of the addressed drive.

Bit 14: ODD CHARACTER. This bit, when set, indicates that the number of characters read in the record was odd.

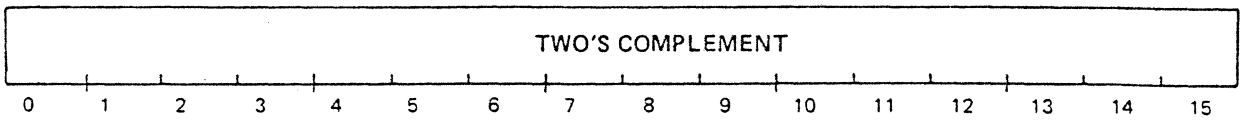
Bit 15: READY. When set, this bit indicates that the addressed drive is idle and ready to accept a command.

Data In B (DIB n,MTA)



The DIB instruction loads the specified accumulator with the contents of the controller's B (memory address) register.

Data In C (DIC n,MTA)



The DIC instruction loads the specified accumulator with the contents of the controller's C (word count) register. The C register word represents the two's complement of either the number of words to be transferred during a read or write operation or the number of records to be spaced over during a space forward or space reverse operation.

3.4.2 I/O Functions

The function, as previously stated, is determined by the states of bits 8 and 9 of the instruction word. Any of the I/O operations can include a function; or a function can be an independent command, without an associated operation (NIO) and without involving an accumulator. The I/O functions are implemented as follows:

F=00 (NIO)	No action. If combined with an associated I/O operation, perform the operation as indicated by bits 5, 6 and 7, but do not initiate command execution.
F=01 (NIOS)	Start (mnemonic S). If combined with an I/O operation, perform the associated operation and execute the command. Set Busy for the duration of command execution. When complete, clear Busy and set Done.
F=10 (NIOC)	Clear (mnemonic C). Stop any current operation. Clear Busy and Done and all registers.
F=11 (NIOP)	Pulse (mnemonic P). Not used.

3.4.3 Command Execution

When the controller receives an isolated (NIOS) or coupled (DOAS, etc.) START command, it will execute the command specified by bits 10, 11 and 12 of the A (command) register as follows.

READ (command 0_8)

The controller places the addressed drive in the read mode and starts the tape in the forward direction. The characters read are assembled into 16-bit words (2 or 3 characters per word) and transferred into the computer through the data channel. The core location of the first word transferred and the number of words to be transferred are determined by the contents of B and C registers respectively.

The data transfer is terminated at the end of a record or when the number of words specified by the C register has been transferred. If the C register specifies fewer words than are contained in the record, the remainder of the record will not be read. If the record contains less words than specified by the C register, the transfer will terminate at the end of the record and the two's complement of the remaining number of words to be read will remain in the C register following the transfer. The controller will always stop the tape in an inter-record gap.

If the number of characters transferred is odd, the controller will place the odd character in bits 0-7, force bits 8-15 to zero and set status bit S14 (Odd Character).

REWIND (command 1_8)

The controller rewinds the addressed drive. If no illegal condition exists, the tape will rewind to the load point (BOT) marker. If an illegal condition exists when the rewind command is issued, the controller will set S3 (Illegal) and subsequently go Done. The Rewind command itself will not set Busy or Done.

OFF-LINE (command 2_8)

The controller places the addressed drive off-line, disabling the drive and all drive status lines. Once a drive has been placed off-line, it can only be placed on-line again from its front panel. The Off-Line command does not set Busy or Done.

SPACE FORWARD (command 3_8)

The controller advances the tape forward one or more records, but transfers no data. The number of records to be spaced over is determined by the contents of the C register. Spacing will continue until the C register overflows (increments to zero) or an end-of-file mark is encountered (an end-of-file mark will not increment the C register). The controller will go Busy for the duration of the operation and then go Done.

SPACE REVERSE (command 4_8)

The controller reverses the tape one or more records but does not transfer data. The number of records to be spaced over is determined by the contents of the C register. Spacing continues until either the C register overflows, the load-point (BOT) marker is reached, or an end-of-file mark is encountered (the end-of-file mark will not increment the C register). If the space reverse command is issued when the tape is beyond the end-of-tape marker, the End-of-Tape status bit (S6) will not be set.

WRITE (command 5_8)

The controller places the addressed drive into the write mode, starts the tape in the forward direction and begins writing data on the tape. The memory location of the first data word written and the number of words to be written are determined by the contents of the B and C registers respectively. When the specified number of words have been transferred, the controller erases a 0.6 inch (9-track) or 0.75 inch (7-track) gap (IRG) on the tape. The controller always writes an integral number of words from core with the shortest legitimate data record therefore consisting of two characters. The controller goes Busy for the duration of the transfer and goes Done when the transfer is complete.

WRITE EOF (command 6_8)

The controller starts the addressed drive, erases 3.9 inches (7-track) or

3.75 inches (9-track) writes an End-of-File mark and sets End-or-File status bit (S7).

ERASE (command 7_8)

The controller erases 6 inches of tape on the addressed drive and then goes Done.

3.5 CPU CONVENTIONS

The 3120 controller responds to the following CPU instructions.

3.5.1 IORST Command

The IORST (I/O Reset) command resets the controller's A, B and C registers, all control logic and all status register bits not derived directly from the drive. Any operation in progress is terminated immediately, clearing both Busy and Done.

3.5.2 Interrupt Commands

The controller responds to INTA and MSKO commands. The standard mask bit is 1Ø.

3.5.3 Flag Checking Commands.

The controller responds to SKPBZ, SKPBN, SKPDZ and SKPDN commands addressed to device code 22_8 (MTA).

SECTION 4
THEORY OF OPERATION

4.1 INTRODUCTION

This section describes and explains the operation of the 3120 Tape Controller. Section 4.2 describes the operation of each logical block while Section 4.3 relates the operation of the individual blocks into an overall description of the basic control cycles.

The level of the following discussion assumes that the reader has a basic knowledge of digital electronics. As a prerequisite, the reader should be familiar with the computer instruction set and the controller's command set and data format as outlined in Section 3 of this manual. Familiarity with the tape drive interface specifications and operation will also prove beneficial to the comprehension of controller operation.

4.1.1 Device Identification

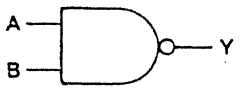
The controller logic card schematic (drawing 96-0204214-1) consists of twenty-nine individual schematic drawings which are labeled sheets 3 through 31 (inclusive) and are contained in Section 6 of this manual. Sheet 2 of the schematic is the interconnect logic diagram which defines the input/output signal paths between the various logical blocks. Subsection title blocks, identifying the circuit description, include the corresponding schematic sheet reference number. Each circuit component will be identified by its integrated circuit location and prime output such as E8-5, the STRT DLAY flip-flop. When the discussion references a component located on another sheet of the schematics, the sheet number will be enclosed in parentheses immediately preceding the circuit location such as (11) B7-9, indicating that the component referenced (B7-9) can be found on sheet 11.

The integrated circuit locations (E8, B7, etc.) on the schematic drawings are referenced to the logic card component location illustration in Section 6. Components are arranged on a 12 by 16 matrix. The alpha reference defines the

vertical column (A through N, omitting G and I) while the numeric reference defines the horizontal row (1-16). An integrated circuit referenced E8 would therefore indicate the eighth (down) integrated circuit appearing in column E.

4.1.2 Logic Conventions

Schematic logic symbols use the "active state" convention in the positioning of the inversion symbol. A gate with the inversion symbol on its output indicates the output is active in its low (Ø volt) state while a gate without an inversion symbol at its output indicates the output is active in its high state. Logic symbols are drawn according to their circuit function rather than the manufacturer's definition. As an example, a gate defined as NAND by the manufacturer could be represented in either of the two following configurations depending on its application.



A	B	Y
L	L	H
H	L	H
L	H	H
H	H	L

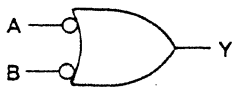


FIGURE 4-1
LOGIC CONVENTIONS

The gate configuration on the left indicates that the desired low level output results from a logic high level at both inputs (AND function) while the gate configuration on the right indicates the desired high level output results from either (or both) input being at a logic low level (OR function).

In addition to the inversion symbol convention, output signal nomenclature also follows an active state convention. A signal (or level) without the "not bar" (e.g., BUSY) indicates a positive state active signal while a signal noted with the "not bar" (e.g., $\overline{\text{BUSY}}$) indicates a negative state active signal.

4.1.3 Signal Acronyms

A majority of the input/output signals appearing on the schematics are acronyms (abbreviations) of their specific function. The following table (Table 4-1) lists, in alphabetical order, the acronym, corresponding signal name and the schematic sheet number for the origin and destination(s) of the signal.

NOTE

Signals designating "Drive" as their origin or destination are interfaced through the I/O adaptor assembly (refer to sheets 2 and 3 of I/O adapter schematic 96-0204252-5).

TABLE 4-1
ACRONYMS

ACRONYM	NAME	ORIGIN	DESTINATION
ALT DEV CODE	Alternate Device Code	13	3
BCLR	Busy Clear	12	8, 14
$\overline{\text{BLCR}}$	Busy Clear	12	8, 9, 16, 17, 19, 20, 27, 28
BDE	Begin Data Entry	8	20, 23
BHDI	High Density Indicator	28	20, 30
$\overline{\text{BHDI}}$	High Density Indicator	28	20
BUSY	Busy	12	11
$\overline{\text{BUSY}}$	Busy	12	30
CHARØ	Character Ø	15	16
CHAR2	Character 2	15	14
$\overline{\text{CHAR3}}$	Character 3	15	14
CLR	Clear	Nova	4
$\overline{\text{CLR}}$	Clear	4	12

TABLE 4-1 (Continued)

ACRONYM	NAME	ORIGIN	DESTINATION
CM1	Command Bit 1	6	7, 10
CM2	Command Bit 2	6	7, 10
CM4	Command Bit 4	6	7, 10
CRC ENABLE	CRC Enable	20	22
$\overline{\text{CRC ENABLE}}$	CRC Enable	20	22
CRCK	CRC Clock	20	24
$\overline{\text{CRCP}}$	CRC Parity	24	22
$\overline{\text{CRCØ}}$	CRC Ø	24	22
$\overline{\text{CRC1}}$	CRC 1	24	22
CRC2	CRC 2	24	22
$\overline{\text{CRC3}}$	CRC 3	24	22
CRC4	CRC 4	24	22
$\overline{\text{CRC5}}$	CRC 5	24	22
$\overline{\text{CRC6}}$	CRC 6	24	22
$\overline{\text{CRC7}}$	CRC 7	24	22
CØ	Command Read	7	15, 17
$\overline{\text{CØ}}$	Command Read	7	8, 14, 29
CØ+C5	Command Read or Write	7	23
C1	Command Rewind	7	11, 12
C2	Command Off Line	7	12
C3+C4	Command Space Forward or Space Reverse	7	8, 19
C4	Command Space Reverse	7	8, 11, 12, 30
$\overline{\text{C4}}$	Command Space Reverse	7	8
C5	Command Write	7	6, 12, 15
$\overline{\text{C5}}$	Command Write	7	14
C5+C6	Command Write or Write EOF	7	8, 20
$\overline{\text{C5+C6}}$	Command Write or Write EOF	7	12
C6	Command Write EOF	7	20, 22
$\overline{\text{C6}}$	Command Write EOF	7	20, 22
C7	Command Erase	7	8
$\overline{\text{C7}}$	Command Erase	7	12

TABLE 4-1 (Continued)

ACRONYM	NAME	ORIGIN	DESTINATION
DATAØ-DATA15	Data Bits Ø-15	Nova	3
$\overline{\text{DATAØ-DATA15}}$	Data Bits Ø-15	3	Nova
DATIA	Data In A	Nova	4
$\overline{\text{DATIA}}$	Data In A	4	5
DATIB	Data In B	Nova	4
$\overline{\text{DATIB}}$	Data In B	4	5
DATIC	Data In C	Nova	4
$\overline{\text{DATIC}}$	Data In C	4	5
DATOA	Data Out A	Nova	4
$\overline{\text{DATOA}}$	Data Out A	4	5
DATOB	Data Out B	Nova	4
$\overline{\text{DATOB}}$	Data Out B	4	5
DATOC	Data Out C	Nova	4
$\overline{\text{DATOC}}$	Data Out C	4	5
DCHA	Data Channel Acknowledge	4	17
$\overline{\text{DCHA}}$	Data Channel Acknowledge	Nova	4
DCHI	Data Channel In	Nova	4
$\overline{\text{DCHI}}$	Data Channel In	4	17
DCHMØ	Data Channel Mode Ø	17	3
$\overline{\text{DCHMØ}}$	Data Channel Mode Ø	3	Nova
DCHM1 (ØV)	Data Channel Mode 1	3	Nova
DCHO	Data Channel Out	Nova	4
$\overline{\text{DCHO}}$	Data Channel Out	4	17
DCHP-IN	Data Channel Priority In	4	17
$\overline{\text{DCHP-IN}}$	Data Channel Priority In	Nova	4
DCHP-OUT	Data Channel Priority Out	17	3
$\overline{\text{DCHP-OUT}}$	Data Channel Priority Out	3	Nova
DCHR	Data Channel Request	17	3
$\overline{\text{DCHR}}$	Data Channel Request	3	Nova
$\overline{\text{DCH REQ}}$	Request Data Channel	14	17
DELD RGAP	Delayed Record Gap	28	19
DENSITY LOW	Density Low	6	25

TABLE 4-1 (Continued)

ACRONYM	NAME	ORIGIN	DESTINATION
$\overline{\text{DENSITY LOW}}$	Density Low	6	5, 28
DEV CODE	Device Code	13	3
DEV SELG	Device Select Gated	5	12
$\overline{\text{DEV SELG}}$	Device Select Gated	5	12
DLDP	Delayed Load Point	8	10, 12, 30
DONE	Done	12	13
DSØ-DS5	Device Select Bits Ø-5	4	5
$\overline{\text{DSØ-DS5}}$	Device Select Bits Ø-5	Nova	4
DSDCHO	Device Select Data Channel Out	17	21
DSTRT	Delayed Start	12	11
$\overline{\text{EDIT}}$	Edit	6	25
$\overline{\text{EDITD}}$	Edit Drive	25	Drive
ENABLED RDS	Enabled Read Strobe	23	28, 29
ENPAR	Enable Parity	22	24
$\overline{\text{EOF}}$	End-of-File	30	19
$\overline{\text{EOF DET}}$	End-of-File Detect	29	8, 30
EOR 2	End-of-Record 2	28	14
$\overline{\text{EOR 2}}$	End-of-Record 2	28	23
EOT	End-of-Tape	26	30
$\overline{\text{EOT}}$	End-of-Tape	Drive	26
EVEN PARITY	Even Parity	6	22, 29
$\overline{\text{EVEN PARITY}}$	Even Parity	22	29
$\overline{\text{FIRST CHAR}}$	First Character	28	30
FPT	File Protect	26	30
$\overline{\text{FPT}}$	File Protect	Drive	26
GRDS	Gated Read Strobe	29	14, 16, 30
$\overline{\text{G STRT}}$	Go Start	11	8

TABLE 4-1 (Continued)

ACRONYM	NAME	ORIGIN	DESTINATION
HDC	High Density Clock	9	10, 20
HDI	High Density Indicator	26	5
$\overline{\text{HDI}}$	High Density Indicator	Drive	26
$\overline{\text{HDSD}}$	High Density Select Drive	25	Drive
IDATA Ø-IDATA 5	Data In Bits Ø-5	3	18, 21
IDATA 6-IDATA 15 (except IDATA 1Ø)	Data In Bits 6-15 (except Bit 1Ø)	3	6, 18, 21
IDATA 1Ø	Data In Bit 1Ø	3	6, 13, 18, 21
$\overline{\text{ILLSTRT}}$	Illegal Start	12	30
INTA	Interrupt Acknowledge	Nova	4
$\overline{\text{INTA}}$	Interrupt Acknowledge	4	13
INTP-IN	Interrupt Priority In	4	13
$\overline{\text{INTP-IN}}$	Interrupt Priority In	Nova	4
INTP-OUT	Interrupt Priority Out	13	3
$\overline{\text{INTP-OUT}}$	Interrupt Priority Out	3	Nova
INTR	Interrupt Request	13	3
$\overline{\text{INTR}}$	Interrupt Request	3	Nova
IOPLS	I/O Pulse	Nova	4
$\overline{\text{IOPLS}}$	I/O Pulse (not used)	4	-
IORST	I/O Reset	Nova	4
$\overline{\text{IORST}}$	I/O Reset	4	12, 13, 19
$\overline{\text{IORST 2}}$	I/O Reset 2	19	18
K3, LINK c	(special application)	26	-
K3, LINK c	(special application)	Drive	26
$\overline{\text{LCCE}}$	Longitudinal Check Character Error	23	30
$\overline{\text{LCRCK}}$	Longitudinal Parity Clock	20	22
LDC	Low Density Clock	9	20
LDP	Load Point	26	8
$\overline{\text{LDP}}$	Load Point	Drive	26
$\overline{\text{LRC REG RST}}$	LRC Register Reset	28	23, 29

TABLE 4-1 (Continued)

ACRONYM	NAME	ORIGIN	DESTINATION
MA Ø	Address Register Bit Ø	18	28
MA 1-MA 15	Address Register Bits 1-15	18	31
MD Ø-MD 15	Data Register Bits Ø-15	27	31
MDENS	Multiple Density	5	3
MDENS	Multiple Density	3	Nova
MS Ø-12,14,15	Status Register Bits Ø-12, 14, 15	30	31
MS 13	Status Register Bit 13	30	12, 31
MSKO	Mask Out	4	13
$\overline{\text{MSKO}}$	Mask Out	Nova	4
MW Ø-MW 15	Word Count Register Bits Ø-15	19	31
ODATA Ø-ODATA 15	Data Out Bits Ø-15	31	3
$\overline{\text{ODD}}$	Odd	14	16, 30
$\overline{\text{OFFC}}$	Off-Line Command	12	25
$\overline{\text{OFFCD}}$	Off-Line Command Drive	25	Drive
$\overline{\text{PCCR}}$	Power Clear Reset	12	13, 30
$\overline{\text{PESEL}}$	PE Select	5	22
RD Ø-RD 7	Read Data Bits Ø-7	26	23, 27, 29
$\overline{\text{RD Ø-RD 7}}$	Read Data Bits Ø-7	Drive	26
RDP	Read Data Parity	26	23, 29
$\overline{\text{RDP}}$	Read Data Parity	Drive	26
RDS	Read Strobe	26	23
$\overline{\text{RDS}}$	Read Strobe	Drive	26
$\overline{\text{RDS 1}}$	Read Strobe 1	23	27, 29
RD/WRT SHFT	Read/Write Shift	16	21, 27
RDY	Ready	26	12, 30
$\overline{\text{RDY}}$	Ready	Drive	26
REG ADV	Register Advance	19	18
RGAP	Record Gap	28	8, 29, 30
RQENB	Request Enable	4	13, 17
$\overline{\text{RQENB}}$	Request Enable	Nova	4

TABLE 4-1 (Continued)

ACRONYM	NAME	ORIGIN	DESTINATION
RQ SHFT	Request Shift	20	16, 30
$\overline{\text{RST}}$	Reset	12	6, 11
$\overline{\text{RWC}}$	Rewind Command	12	25
$\overline{\text{RWCD}}$	Rewind Command Drive	25	Drive
RWD	Rewinding	26	30
$\overline{\text{RWD}}$	Rewinding	Drive	26
SDATIA	Strobe Data In A	5	31
SDATIB	Strobe Data In B	5	31
SDATIC	Strobe Data In C	5	31
SDATOA	Strobe Data Out A	5	11
$\overline{\text{SDATOA}}$	Strobe Data Out A	11	6
SDATOB	Strobe Data Out B	5	18
SDATOC	Strobe Data Out C	5	19
SDCHA	Strobe Data Channel Acknowledge	17	31
$\overline{\text{SDCHA}}$	Strobe Data Channel Acknowledge	17	19
SDCHI	Strobe Data Channel In	17	14,31
SDCHO	Strobe Data Channel Out	17	14
SELB	Select Busy	12	3
$\overline{\text{SELB}}$	Select Busy	3	Nova
SELD	Select Done	12	3
$\overline{\text{SELD}}$	Select Done	3	Nova
SEND CLOCK	Send Clock	8	30
$\overline{\text{SEND CLOCK}}$	Send Clock	8	10
SET DONE	Set Done	8	12
$\overline{\text{SFC}}$	Stop/Forward Command	8	25
$\overline{\text{SFCD}}$	Stop/Forward Drive Command	25	Drive
SHFT	Shift	16	15
$\overline{\text{SHFT COMPL}}$	Shift Complete	15	14, 16
$\overline{\text{SLT Ø}}$	Select Ø	6	5, 25

TABLE 4-1 (Continued)

ACRONYM	NAME	ORIGIN	DESTINATION
$\overline{\text{SLT 1}}$	Select 1	6	5, 25
$\overline{\text{SLT 2}}$	Select 2	6	5, 25
$\overline{\text{SLT 3}}$	Select 3	6	5, 25
$\overline{\text{SLTD Ø}}$	Select Drive Ø	25	Drive
$\overline{\text{SLTD 1}}$	Select Drive 1	25	Drive
$\overline{\text{SLTD 2}}$	Select Drive 2	25	Drive
$\overline{\text{SLTD 3}}$	Select Drive 3	25	Drive
$\overline{\text{SRC}}$	Stop/Reverse Command	8	25
$\overline{\text{SRCD}}$	Stop/Reverse Drive Command	25	Drive
START DELAY	Start Delay	8	10
$\overline{\text{START DELAY}}$	Start Delay	8	10
STOP	Stop	8	11
$\overline{\text{STOP DELAY}}$	Stop Delay	8	30
STRT	Start	Nova	4
$\overline{\text{STRT}}$	Start	4	12
$\overline{\text{SWS}}$	Write Enable	12	25
$\overline{\text{SWSD}}$	Write Enable Drive	25	Drive
THREE	Three	15	27
$\overline{\text{THREE}}$	Three	15	14
$\overline{\text{TIME OUT}}$	Time Out	10	8
T1	Shift Clock Phase 1	14	16
T2	Shift Clock Phase 2	14	15, 16
$\overline{\text{VRCE}}$	Vertical Parity Error	29	30
WAR	Write Amplifier Reset	20	25
$\overline{\text{WARSD}}$	Write Amplifier Reset Drive	25	Drive
WC=Ø	Word Count = Ø	19	8, 14, 20
$\overline{\text{WC=Ø}}$	Word Count = Ø	19	29, 30
WCHAR Ø-WCHAR 7	Write Character Bits Ø-7	21	22
WD Ø-WD 7	Write Data Bits Ø-7	22	24, 25

TABLE 4-1 (Continued)

ACRONYM	NAME	ORIGIN	DESTINATION
$\overline{\text{WD Ø-WD 7}}$	Write Data Bits Ø-7	25	Drive
WDP	Write Data Parity	22	25
$\overline{\text{WDP}}$	Write Data Parity	25	Drive
$\overline{\text{WRSC}}$	Write Start Command	12	14, 16, 24
$\overline{\text{WRT REG CLR}}$	Write Register Clear	16	21
WDS	Write Data Strobe	20	25
$\overline{\text{WDSD}}$	Write Data Strobe Drive	25	Drive
XF	Transfer Full	14	15, 16
XFR1-2	Transfer 1-2	14	21, 27
1 FULL	1 Full	14	30
$\overline{\text{1 FULL}}$	1 Full	14	20
2 FULL	2 Full	14	30
$\overline{\text{2 FULL}}$	2 Full	14	20, 30
3 CHAR MODE	3 Character Mode	6	15
9T	Nine Track	6	10, 20, 22, 27, 28, 29, 30
$\overline{\text{9T}}$	Nine Track	6	15, 20, 22, 23

The remainder of this section was unavailable at time of printing. Please complete the Manual Correction Request form at the rear of this manual and a complete manual will be sent as soon as it becomes available.

SECTION 5
MAINTENANCE

5.1 INTRODUCTION

Section 5 presents pertinent information regarding the maintenance, troubleshooting and repair of the 3120 Tape Controller. Also contained within this section are integrated circuit equivalent diagrams for each type of integrated circuit employed within the controller as an additional aid in diagnosing component malfunctions.

5.2 RECOMMENDED TEST EQUIPMENT

The following table (Table 5-1) offers a list of suggested test equipment required for analyzing and troubleshooting circuit operation (equivalent equipment acceptable).

TABLE 5-1
RECOMMENDED TEST EQUIPMENT

INSTRUMENT DESCRIPTION	MANUFACTURER AND MODEL	MINIMUM REQUIREMENTS
Volt/Ohm Meter	Triplette Model 630-APL	3%
Oscilloscope	Tektronix Model 465	100MHz bandwidth, dual-trace operation, delayed trigger.
Integrated Circuit Extender Clip	AP Inc. 923-700 or Pomona Electronics 3916	N/A

5.3 REQUIRED TOOLS

The following minimum inventory of tools and supplies are required to adequately repair the controller:

Thermostatically Controlled Soldering Iron
Pneumatic Solder Extractor
Solder, Rosin Core 60/40

Screwdrivers, Phillips-head and Common
Pliers, Diagonal-Cutting
Pliers, Long-Nose

5.4 MAINTENANCE

There are no preventative maintenance requirements for the controller. Periodic maintenance is limited to running the 3120 Tape Exerciser at 90-day intervals to ensure proper operation of the controller. Refer to Exerciser manual.

5.5 CALIBRATION

The 3120 Controller contains no adjustable devices and therefore requires no calibration.

5.6 TROUBLESHOOTING

Troubleshooting of the controller is accomplished in a three-level process. Following familiarzation with the theory of operation (Section 4), the first level in servicing a unit that has failed is to "sectionalize" the fault to a major circuit block. Once traced to a major block, the second level or "localization" of the failure is undertaken to confine the fault to an individual stage or circuit within the major block. The third level or "isolation" involves the actual location of the defective component within the stage that has failed.

In the event of a suspected failure and before any troubleshooting or repairs are attempted, read the Ball Computer Products Warranty Statement. Verify that the malfunction is not attributed to the CPU or tape drive. All other system peripherals should be removed or disconnected to reduce system variables and the controller should be installed in the first available slot above the top memory board. Verify the CPU's operation using the CPU exerciser and memory test. If available, use a known good drive and ensure that the magnetic tape itself is of known good quality. Ensure that the write-

protect ring is installed and that the tape is threaded correctly. Additionally, verify that the correct device code is selected and that the speed selection jumpers and components correspond to the drive in use (refer to Section 2.5.2.1). The remainder of the troubleshooting description will assume that the CPU and drive are operating correctly.

If a valid malfunction is encountered, first ensure that the 5 volt dc power level is present and correct before attempting to sectionalize the malfunction. Referring to Figure 5-1, the 5 volt level can be measured at the GND and VCC test points at the right-hand corner of the logic card. Connect the voltmeter's low (common) lead to GND and the high lead to VCC. The correct reading should be between 4.8 and 5.2 volts.

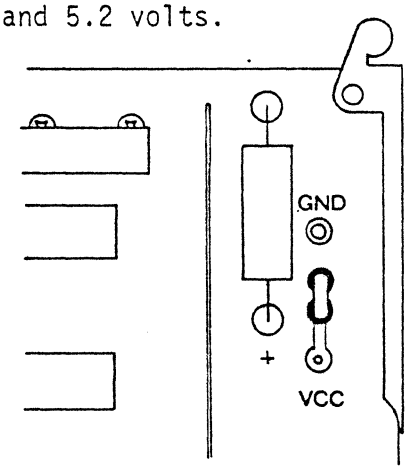


FIGURE 5-1
5 VOLT TEST POINTS

5.6.1 Sectionalization

Sectionalization of a controller malfunction is accomplished using the 3120 Tape Exerciser. Referring to Section 5.7, provide access to the controller logic card as outlined. Load and run the 3120 Tape Exerciser binary tape. Running, or attempting to run, the exerciser program will provide one of the four following indications:

1. No Operation
2. Fatal Error
3. Error Summary
4. Correct Operation

5.6.1.1 No Operation

If there is no response from the exerciser, the tape should be manually advanced past the load point (approximately six feet) and the exerciser again restarted. If, at this time, the exerciser rewinds the tape, the device code select logic is operating and the rewind command decode logic is functional. If the drive fails to rewind the tape, a problem in these areas is indicated.

5.6.1.2 Fatal Error

A "fatal error" occurs when the exerciser program cannot be completed. The exerciser will halt at the operation causing the error and generate the following message on the Teletype:

```
CONTROLLER FAILURE AT xxxxx
AAAAAA    BBBBBB    CCCCCC
```

The interpretation of this message is explained in the 3120 Tape Exerciser manual. Using this information, the operation causing the failure can be determined, indicating the probable area of the malfunction.

5.6.1.3 Error Summary

An error summary is printed following the running of the exerciser or immediately following certain fatal errors. The summary defines both the number and type of errors occurring as a result of the exerciser, indicating the nature of the malfunction. The "interface" errors are especially useful when malfunctions between the CPU and controller are probable and are described on Page A-17 in the 3120 Tape Exerciser Manual.

5.6.1.4 Correct Operation

The successful running of the exerciser indicates that the controller is operating properly. Whenever a component is replaced, the exerciser should again be run to verify that the repair was successful and that no other malfunction exists.

5.6.2 Localization

Localization of the malfunction is accomplished using an oscilloscope and small, user-generated control programs. As an example, assume a fatal error occurred at step 203 of the exerciser program. Referring to the exerciser listing, step 00203 indicates that an "end-of-file" was not recognized or, specifically, the EOF flip-flop was never set. Rather than continually running the exerciser, a small program can be created to perform the write EOF operation and manually loaded into the CPU using the data switches. A program which may be used is:

```
77/  000060          -Write EOF command
100/ NIOC 22         -Clear
101/ LDA 0,77        -Load AC0
102/ DOAS 0,22       -Start
103/ SKPDN 22        -Skip if Done
104/ JMP. -1         -Loop
105/ JMP 100         -Start Again
```

This program will attempt to set the EOF flip-flop. Referring to the theory of operation and the schematic drawings, EOF flip-flop H11-5 on sheet 30 (Status Register) is set directly by the $\overline{\text{EOF DET}}$ signal from D7-8 on sheet 29 (EOF/Vertical Parity Detection Logic). Using the oscilloscope and, if available, the integrated circuit extender clip, monitor the MS7 output at H11-5. Starting the program should, if the circuitry is functioning correctly, result in the setting of the flip-flop. If the flip-flop remains reset, restart the program while monitoring the set input at pin 4 to determine if the $\overline{\text{EOF DET}}$ signal is being generated. If this signal were present, the malfunction would be associated with the flip-flop. Monitoring the reset input at pin 1 would determine if the flip-flop were being held reset by $\overline{\text{PCCR}}$. If the $\overline{\text{EOF DET}}$ signal is not present, continue to trace signal flow back through each circuit, restarting the program each time until the malfunction is located.

5.6.3 Isolation

Isolation of the malfunction is accomplished using an oscilloscope and ohmmeter to determine the actual origin of the problem. The integrated circuit equivalents contained in Section 5.8 should be consulted regarding logic configurations and truth tables.

5.7 LOGIC CARD ACCESS

In order to effectively troubleshoot the controller logic card, complete access to the component side of the card is required. The two methods of accessing the components are either to:

1. Mount the logic card on an extender board.
2. Remove the top cover plate of the CPU and install the logic card in the top available slot.

Prior to removing the logic card from the CPU, ensure that both the CPU and the drive are powered-down. Disconnect the controller-to-adapter interface cables at the logic card edge-connectors using the supplied 3M No. 3438 extractor tool. To unseat the logic card from the back-plane board, pull the ejection levers located at the extremities of the card. Slide the logic card out and, using a screwdriver, remove the three screws securing the protective cover to the top of the logic card.

5.7.1 Extender Board

If an extender board (Data General P/N 107-000007-02, or equivalent) is to be used, insert the extender board into the slot previously occupied by the controller and mount the controller into the extender board connectors.

5.7.2 Cover Plate Removal

If an extender board is not available, the top of the CPU may be removed to provide the necessary access to the controller. Once removed, the controller can be installed in the top available slot, providing access from the top of the CPU.

NOTE

Ensure that the data channel and interrupt priorities are maintained by jumpering the DCHP and INTP IN and OUT signals as described in Section 2.5.1.

5.8 REPAIR TECHNIQUES

Repair of the controller should be undertaken only by qualified personnel adept in solid-state repair techniques. When a component failure is encountered, observe these general instructions:

1. Never remove or replace a component or the logic card while power is applied to the CPU or tape drive.
2. Use only a grounded, transformer-coupled, thermostatically controlled soldering iron.
3. Avoid any application of acid-core type solder.

5.8.1 Integrated Circuit Replacement

The following instructions outline the correct method for the removal and replacement of a defective integrated circuit.

1. Verify that the integrated circuit in question is defective (refer to the integrated circuit equivalents contained in Section 5.9).
2. From the component side of the logic card, carefully clip each lead of the defective integrated circuit at the point where the lead enters the case. Diagonal-cutting pliers should be used.
3. Working from the component side of the logic card, carefully remove each individual lead using a soldering iron and long-nose pliers.
4. Using a soldering iron and solder, carefully fill each hole with additional solder. This will facilitate the complete removal of the solder.

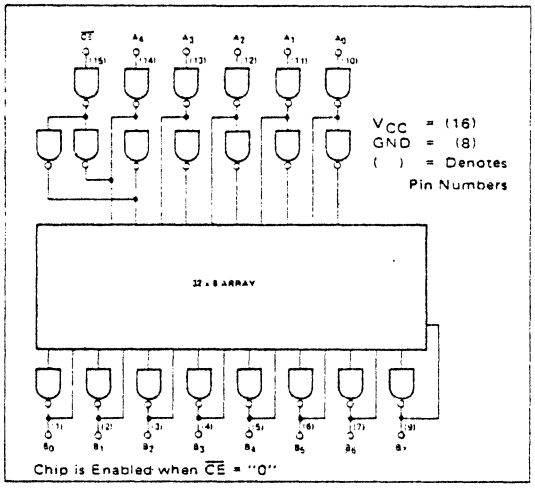
5. Remove the solder from each hole using a pneumatic solder extractor. If, following this operation, solder remains in the hole, repeat Steps 4 and 5.

6. Install the replacement integrated circuit noting correct orientation.

7. From the circuit (bottom) side of the logic card, solder each lead.

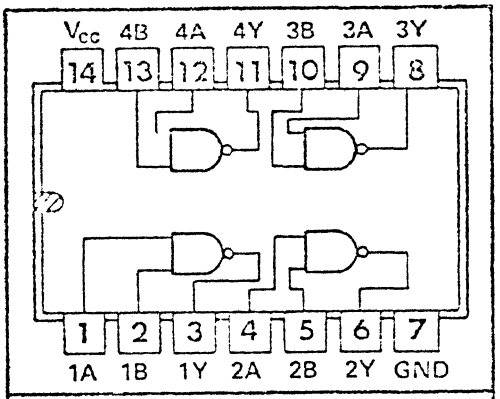
5.9 INTEGRATED CIRCUIT EQUIVALENTS

Circuit equivalents for each type of integrated circuit employed within the controller are described in numerical sequence within this section. If further information is required, refer to the manufacturer's description.



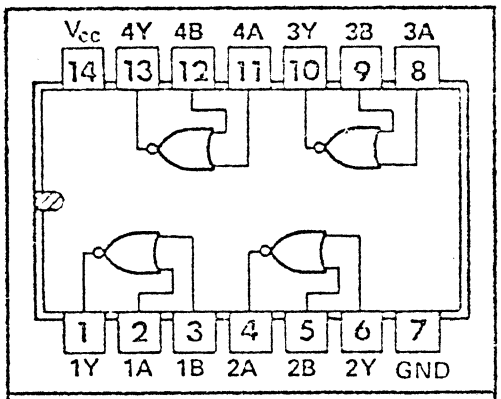
	INPUTS					OUTPUTS							
OCTAL ADDRESS	AØ (1Ø)	A1 (11)	A2 (12)	A3 (13)	A4 (14)	B7 (9)	B6 (7)	B5 (6)	B4 (5)	B3 (4)	B2 (3)	B1 (2)	BØ (1)
Ø	L	L	L	L	L	H	H	H	H	H	H	H	H
1	L	L	L	L	H	L	L	L	L	L	L	L	L
2	L	L	L	H	L	L	L	L	L	L	L	L	L
3	L	L	L	H	H	H	H	H	H	H	H	H	H
4	L	L	H	L	L	H	H	H	H	H	L	H	H
5	L	L	H	L	H	H	H	H	H	H	H	L	H
6	L	L	H	H	L	H	H	H	H	H	H	L	H
7	L	L	H	H	H	H	H	H	H	H	H	L	H
1Ø	L	H	L	L	L	H	H	H	H	H	H	H	H
11	L	H	L	L	H	L	L	L	L	L	L	L	L
12	L	H	L	H	L	L	L	L	L	L	L	L	L
13	L	H	L	H	H	H	H	H	H	H	H	H	H
14	L	H	H	L	L	H	H	H	H	H	H	H	H
15	L	H	H	L	H	H	H	H	H	H	H	L	H
16	L	H	H	H	L	H	H	H	H	H	H	L	H
17	L	H	H	H	H	H	H	H	H	H	H	L	H
2Ø	H	L	L	L	L	H	H	H	H	H	L	L	L
21	H	L	L	L	H	L	L	L	L	L	L	L	L
22	H	L	L	H	L	L	L	L	L	L	L	L	L
23	H	L	L	H	H	H	H	H	H	H	L	L	L
24	H	L	H	L	L	H	H	H	H	H	L	L	H
25	H	L	H	L	H	H	H	H	H	L	H	H	H
26	H	L	H	H	L	H	L	H	H	L	L	L	L
27	H	L	H	H	H	H	L	L	L	L	L	L	L
3Ø	H	H	L	L	L	H	L	H	H	H	H	L	L
31	H	H	L	L	H	L	L	L	L	L	L	L	L
32	H	H	L	H	L	L	L	L	L	L	L	L	L
33	H	H	L	H	H	H	L	H	H	H	H	L	L
34	H	H	H	L	L	L	L	L	L	L	L	L	L
35	H	H	H	L	H	L	H	L	H	H	L	L	L
36	H	H	H	H	L	L	H	L	H	H	L	L	L
37	H	H	H	H	H	L	H	L	H	H	L	L	L

ROM B16 (1756)



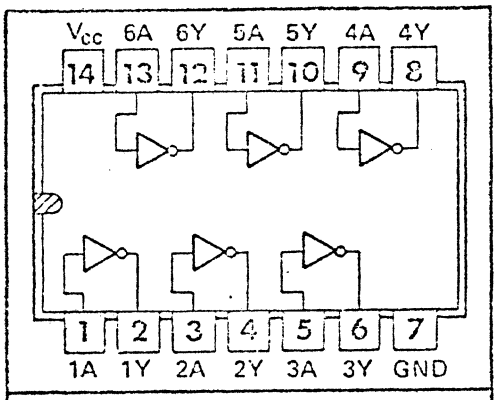
Positive Logic: $Y = \overline{AB}$

7400



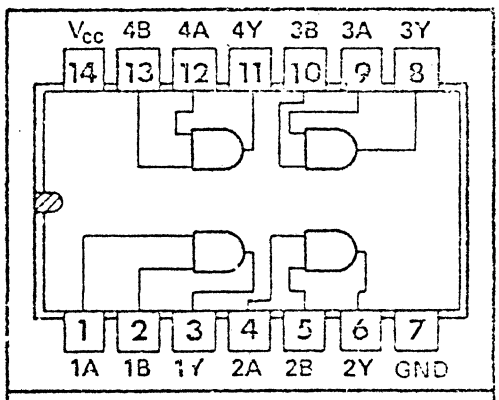
Positive Logic: $Y = \overline{A+B}$

7402



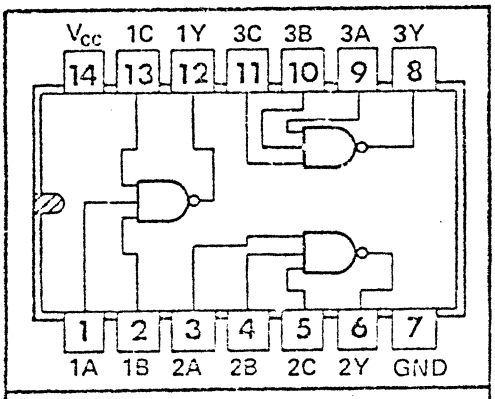
Positive Logic: $Y = \overline{A}$

7404



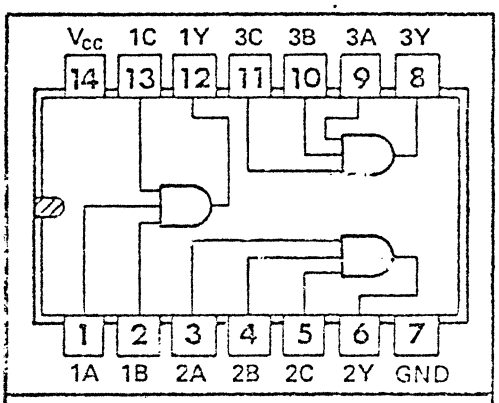
Positive Logic: $Y = AB$

7408



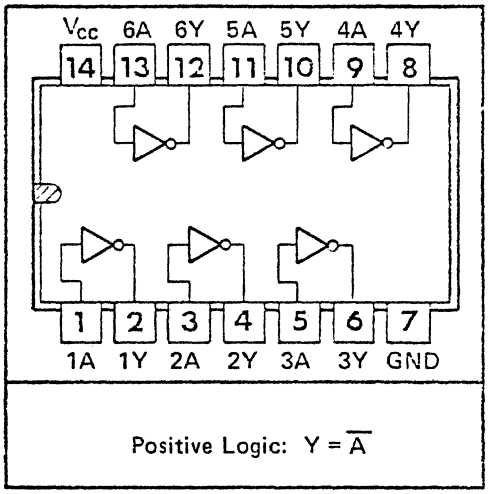
Positive Logic: $Y = \overline{ABC}$

7410

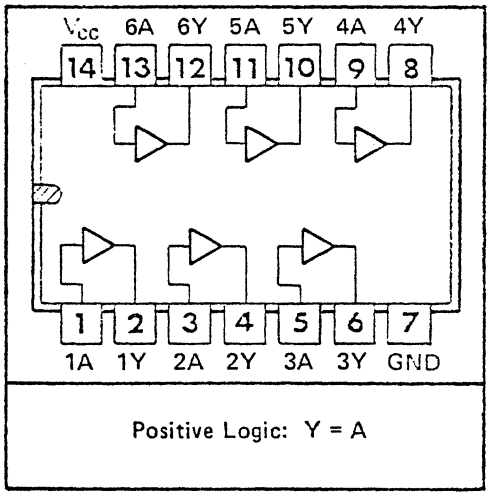


Positive Logic: $Y = ABC$

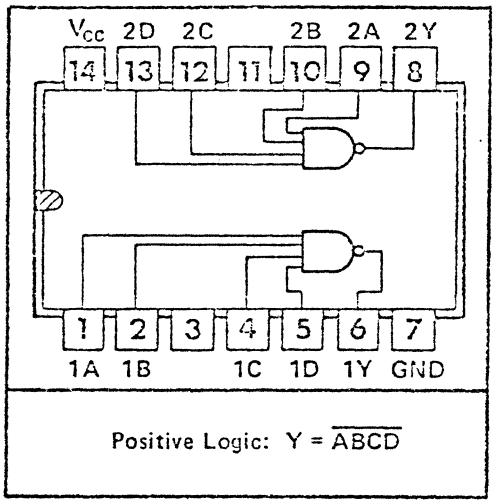
7411



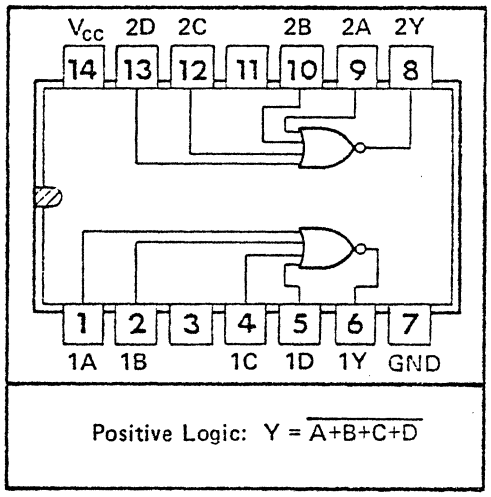
7416



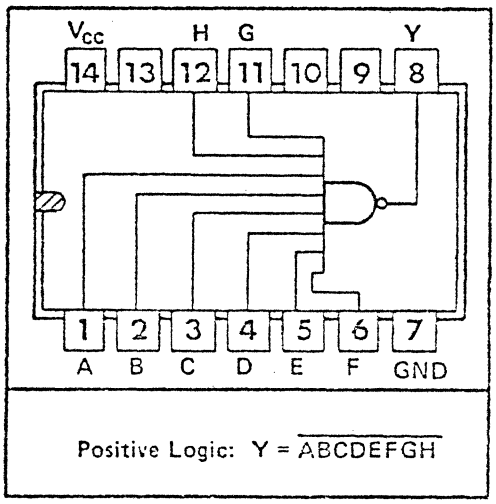
7417



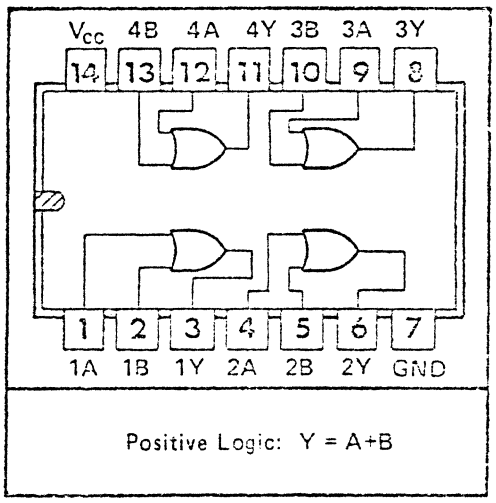
7420



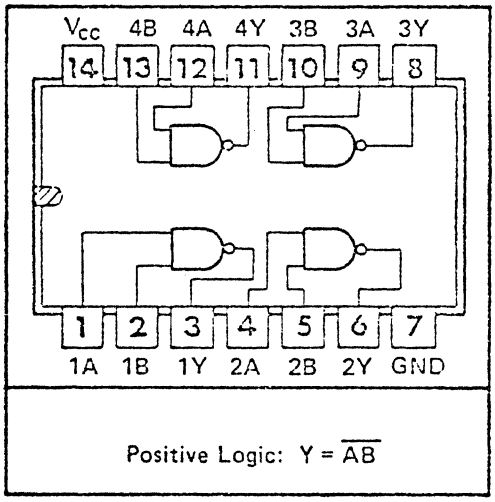
7429



7430



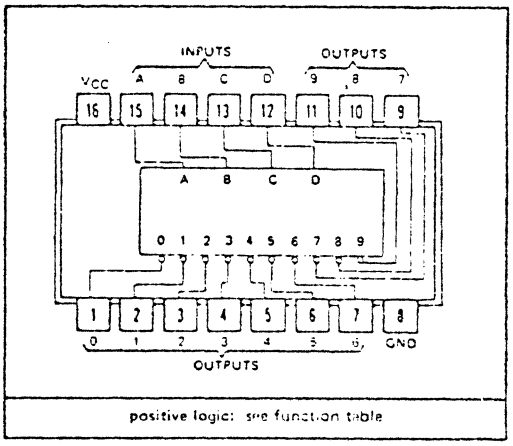
7432



Positive Logic: $Y = \overline{AB}$

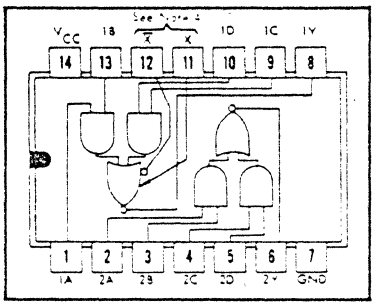
7437/7438

NO	'42A, 'L42 BCD INPUT				ALL TYPES DECIMAL OUTPUT									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H



positive logic: see function table

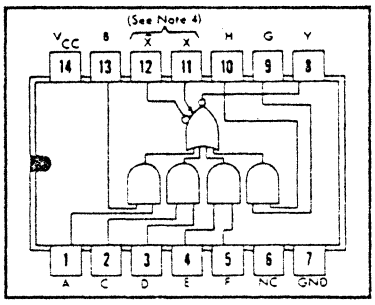
7442



positive logic: $Y = \overline{(AB) \cdot (CD) \cdot (X)}$

X = Output of SN5460/SN7460

7451



positive logic: $Y = \overline{(AB) \cdot (CD) \cdot (EF) \cdot (GH) \cdot (X)}$

X = Output of SN5460/SN7460

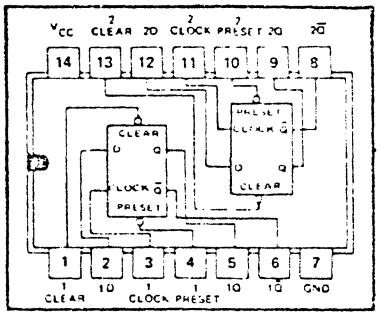
7454

TRUTH TABLE (Each Flip-Flop)

t_n	t_{n+1}	
INPUT D	OUTPUT Q	OUTPUT $\bar{Q}$
0	0	1
1	1	0

NOTES: 1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.

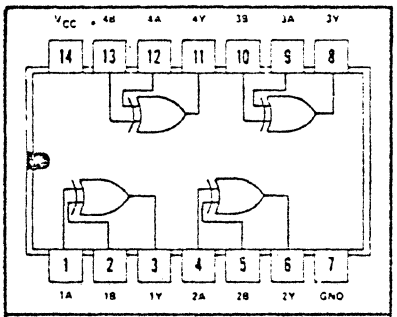
positive logic: Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock



7474

TRUTH TABLE

INPUTS		OUTPUT
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0



positive logic: $Y = A \oplus B$

7486

TRUTH TABLES

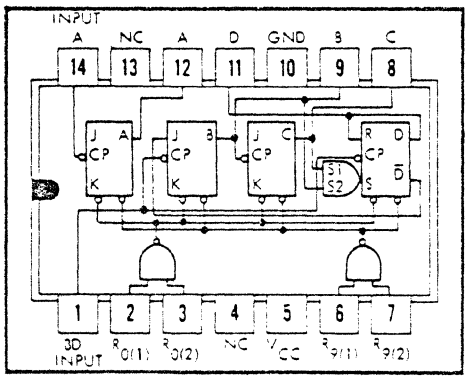
BCD COUNT SEQUENCE
(See Note 1)

COUNT	OUTPUT D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

RESET/COUNT (See Note 2)

RESET INPUTS $R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	OUTPUT D C B A
1	1	0	X	0 0 0 0
1	1	X	0	0 0 0 0
X	X	1	1	1 0 0 1
X	0	X	0	COUNT
0	X	0	X	COUNT
0	X	X	0	COUNT
X	0	0	X	COUNT

NC—No Internal Connection

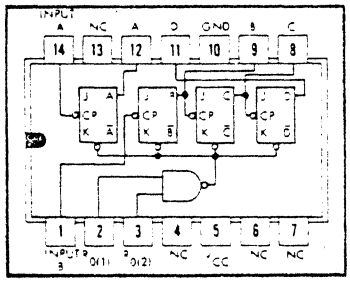


NOTES: 1. Output A connected to input BD for BCD count.
2. X indicates that either a logical 1 or a logical 0 may be present.

7490

TRUTH TABLE (See Notes 1, 2, and 3)

COUNT	OUTPUT D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1



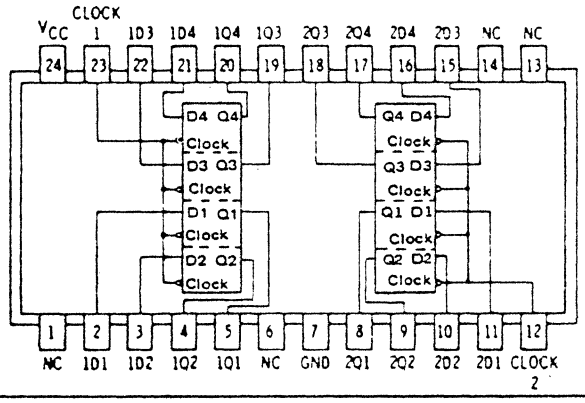
NOTES: 1. Output A connected to input B
2. To reset all outputs to logical 0 both $R_{0(1)}$ and $R_{0(2)}$ inputs must be at logical 1.
3. Either (or both) reset inputs $R_{0(1)}$ and $R_{0(2)}$ must be at a logical 0 to count.

7493

TRUTH TABLE (Each Latch)	
t_n	t_{n+1}
D	Q
1	1
0	0

NOTES: 1. t_n = bit time before clock negative-going transition.
2. t_{n+1} = bit time after clock negative-going transition.

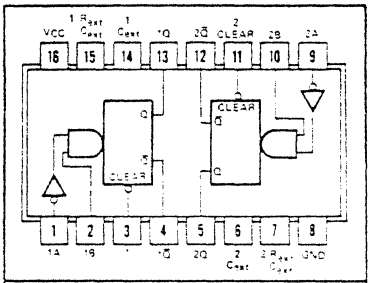
NC—No internal connection



positive logic: see truth table

74100

INPUTS A	B	OUTPUTS Q	$\overline{Q}$
H	X	L	H
X	L	L	H
L	↑	⎍	⎎
↓	H	⎍	⎎

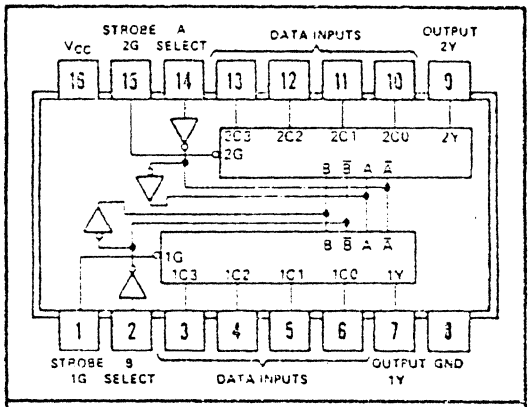


positive logic:
Low input to clear resets Q to low level and inhibits data inputs

74123

TRUTH TABLE

ADDRESS INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

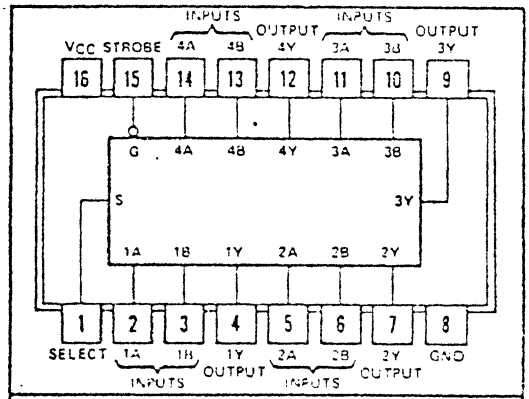


positive logic: See truth table

74153

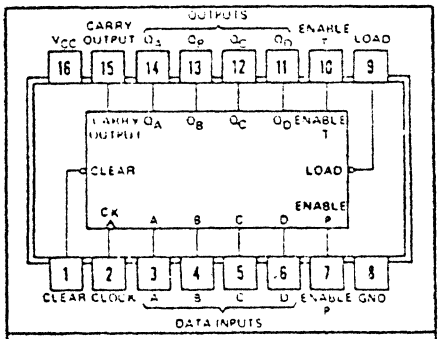
TRUTH TABLE

INPUTS			OUTPUT
STROBE	SELECT	A B	Y
H	X	X X	L
L	L	L X	L
L	L	H X	H
L	H	X L	L
L	H	X H	H



positive logic:
Low logic level at S selects A inputs.
High logic level at S selects B inputs.

74157



positive logic: see description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting schemes. The '160 and '162 are decade counters and the '161 and '163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four J-K master-slave flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. Low-to-high transitions at the load input should be avoided when the clock is low if the enable inputs are high at or before the transition. The clear function for the '160 and '161 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the clock, load, or enable inputs. The clear function for the '162 and '163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the carry output. The carry output thus enabled will produce a positive output pulse with a duration approximately equal to the positive portion of the Q_A output. This positive overflow carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the enable P or T inputs should occur only when the clock input is high.

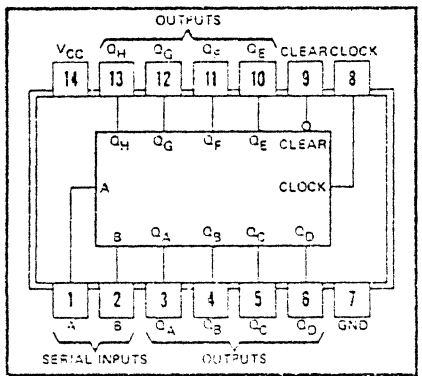
All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design. A full fan-out to ten normalized Series 54/74 loads is available from each of the outputs in the low-level state. A fan-out to 20 normalized Series 54/74 loads is provided in the high-level state to facilitate connection of unused inputs to used inputs. Input clock frequency is typically 32 megahertz and power dissipation is typically 325 milliwatts.

Series 54 circuits are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74 circuits are characterized for operation from 0°C to 70°C.

74161

TRUTH TABLE
SERIAL INPUTS A AND B

INPUTS AT t_n		OUTPUT AT t_{n+1}
A	B	Q_A
H	H	H
L	H	L
H	L	L
L	L	L

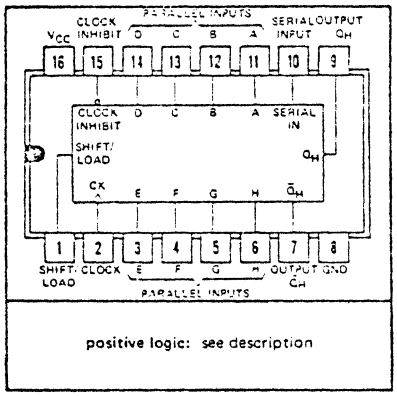


Low input to clear resets all outputs to the low level.

74164

FUNCTION TABLE

INPUTS					INTERNAL OUTPUTS		OUTPUT
SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . . H	Q_A	Q_B	Q_H
L	X	X	X	a . . . h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}



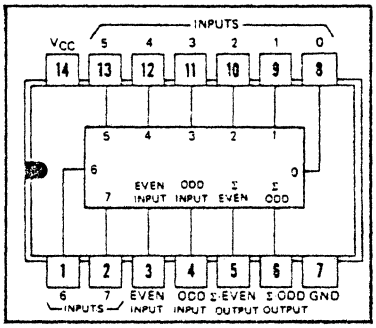
positive logic: see description

74165

TRUTH TABLE

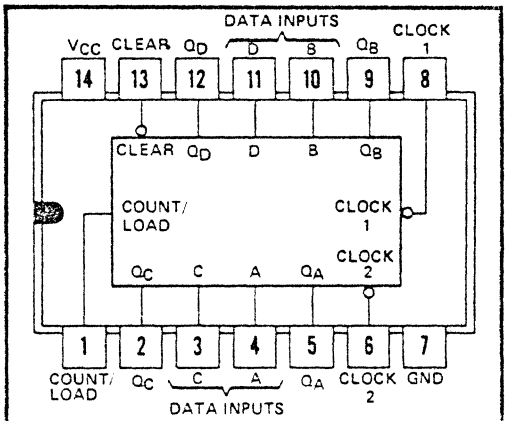
INPUTS			OUTPUTS	
Σ OF 1's AT 0 THRU 7	EVEN	ODD	Σ EVEN	Σ ODD
EVEN	1	0	1	0
ODD	1	0	0	1
EVEN	0	1	0	1
ODD	0	1	1	0
X	1	1	0	0
X	0	0	1	1

X= irrelevant



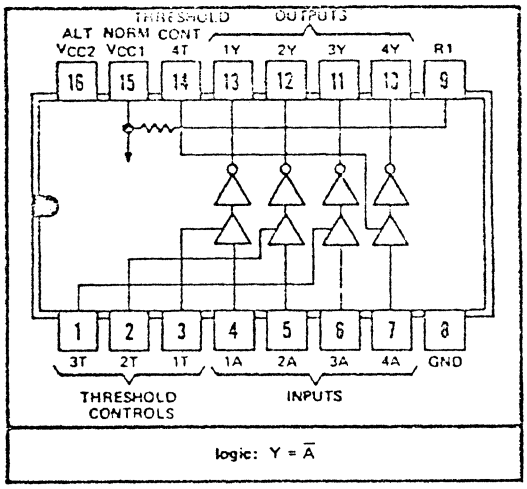
74180

COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H



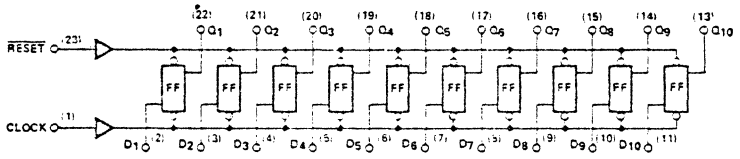
asynchronous input: Low input to clear sets Q_A, Q_B, Q_C and Q_D low.

74197


THRESHOLD
OUTPUTS
ALT NORM CONT
VCC2 VCC1 4T 1Y 2Y 3Y 4Y R1
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
3T 2T 1T 1A 2A 3A 4A GND
THRESHOLD CONTROLS
INPUTS
logic: Y = $\overline{A}$

75154

10-BIT BUFFER REGISTER



D_n	$\overline{RESET}$	Q_{n+1}
1	1	1
0	1	0

$\overline{RESET} = 0 \Rightarrow Q = 0$
(OVERRIDES CLOCK)
n IS TIME PRIOR TO CLOCK
n+1 IS TIME FOLLOWING CLOCK

V_{CC} = (24)
GND = (12)
( ) = Denotes Pin Numbers

8202

8202

5.10 PARTS LIST

This section contains the necessary information for the procurement of replacement parts directly from commercial sources. Individual components are arranged in alpha-numeric succession. To obtain information relating to a specific component, locate the component using the left-hand "reference" column. Component manufacturer's names have been abbreviated in the parts list with either a two-, three- or four-character code. The following table (Table 5-2) cross-references the abbreviation with the full name and address of the prime commercial source.

TABLE 5-2

CODE LIST OF MANUFACTURERS

ABBREVIATION	NAME/ADDRESS
AB	Allen-Bradley Co., Milwaukee, Wisconsin
AVX	AVX Ceramics, Myrtle Beach, South Carolina
BCP	Ball Computer Products Inc., Sunnyvale, California
BECK	Beckman Instruments Inc., Fullerton, California
CGW	Corning Glass Works, Corning, New York
ERIE	Erie Technological Products, Erie, Pennsylvania
ITT	ITT Semiconductors, West Palm Beach, Florida
MMM	Minnesota Mining & Manufacturing Co., St. Paul, Minnesota
SIG	Signetics Corp. Sunnyvale, California
SPR	Sprague Electric Co., North Adams, Massachusetts
TI	Texas Instruments, Dallas, Texas
XTN	X-tron-Electronics Inc., Hayward, California

REFERENCE	DESCRIPTION	PRIME MFR.	MFR. PART NO.	QTY.
C1,14,15, 21,44,46	Capacitor, Ceramic 0.33µF, 50 wvdc	ERIE	8131-Ø5Ø-651-334M	6
C2,13,16, 20,43,45	Capacitor, Electrolytic 100µF, 10 wvdc	SPR	15ØD1Ø7X9Ø1ØR2	6
C3-12, 17-19, 22-24, 28,40	Capacitor, Ceramic 100pF, 200 wvdc	ERIE	CKØ5BX1Ø1K	18
C25,26	Capacitor, Ceramic 470pF, 200 wvdc	ERIE	CKØ5BX471K	2
C27	Capacitor, Electrolytic 56µF, 10 wvdc	SPR	15ØD566X9Ø1ØR2	1
C29	Capacitor, Electrolytic 150µF, 15 wvdc	SPR	15ØD157X9Ø15R2	1
C30	Capacitor, Electrolytic 33µF, 10 wvdc	SPR	15ØD336X9Ø1ØR2	1
C31-34, 38,42,48	Capacitor, Ceramic 0.001µF, 200 wvdc	ERIE	CKØ5BX1Ø2K	7
C35	See Tape Speed Components			
C36	See Tape Speed Components			
C37	Capacitor, Ceramic 200pF, 200 wvdc	ERIE	CKØ5BX221K	1
C39,47	Capacitor, Ceramic 0.0022µF, 100 wvdc	ERIE	CKØ5BX222K	2
C41	See Tape Speed Components			
CR1,2,3,4	Diode, 1N4148	ITT	1N4148	4
Q1	Transistor, 2N3565	TI	2N3565	1
R1-16, 25,26, R30-37, R40-46, 48,49, R51-R64	Resistor, Carbon Comp. 1K, ½W, 5%	AB	CB1Ø25	45

REFERENCE	DESCRIPTION	PRIME MFR.	MFR. PART NO.	QTY.
R17,18, 23,24	Resistor, Carbon Comp. 220Ω, ¼W, 5%	AB	CB2215	4
R19-22, 28	Resistor, Carbon Comp. 330Ω, ¼W, 5%	AB	CB3315	5
R27,50	Resistor, Carbon Comp. 8.2k, ¼W, 5%	AB	CB8225	2
R29	Resistor, Carbon Comp. 22Ω, ¼W, 5%	AB	CB22Ø5	1
R38,39,47	See Tape Speed Components			

INTEGRATED CIRCUITS

REFERENCE	DESCRIPTION	PRIME MFR.	MFR. PART NO.	QTY.
A1,A9,B1, C8,F7,H2, H10,K6,L1, L2	Integrated Circuit, SN7402N Quad 2-Input NOR Gate	TI	SN74Ø2N	10
A2,A3,A4, A8,D6,E2, E5,F5,J7, J8,J9,J13, J16,K4,K12, L12,M12	Integrated Circuit, SN7400N Quad 2-Input NAND Gate	TI	SN74ØØN	17
A5,A7, A13,B1A,B2A, B5,B13,B14, E7,H3,H9, H16,J2,J14, K7,K11,L5, L8,L13,M11, N3,N4,N6, N8	Integrated Circuit, SN7404N Hex Inverter	TI	SN74Ø4N	24
A6,A10,A11, A12,A14,B11, B12	Integrated Circuit, SN7438N Quad 2-Input NAND Buffer	TI	SN7438N	7
A15,B15,C13, C14,D13,D14, E13,E14,F13, F14	Integrated Circuit, SN74197N Binary Counter/Latch	TI	SN74197N	10
A16	Integrated Circuit Package 1k Resistance Network	BECK	899-1-R1.ØK	1
B2,D9,E3, E6,M8	Integrated Circuit, SN7432N Quad 2-Input OR Gate	TI	SN7432N	5
B3,F16	Integrated Circuit, SN7490N Decode Counter	TI	SN749ØN	2
B4,H13,M6	Integrated Circuit, SN7430N 8-Input NAND Gate	TI	SN743ØN	3
B6,B9,E4, F3,H14,J6, K3,K5,K10, K16	Integrated Circuit, SN7408N Quad 2-Input AND Gate	TI	SN74Ø8N	10

INTEGRATED CIRCUITS

REFERENCE	DESCRIPTION	PRIME MFR.	MFR. PART NO.	QTY.
B7,B8,C6, C7,D1,D2, D3,D4,D5, D16,E8,F1, F2,H5,H11, H12,J5,J11, J12,K1,K8, L4,L10,M10	Integrated Circuit, SN7474N Dual Type-D Flip-Flop	TI	SN7474N	24
B10	Integrated Circuit, SN7493N 4-Bit Binary Counter	TI	SN7493N	1
B16	Integrated Circuit, 1756 ROM(Programmed)	BCP	96-Ø9Ø1756-4	1
C3,C4,C5, F4,K2	Integrated Circuit, SN74161N Synchronous 4-Bit Counter	TI	SN74161N	5
C9,E9,M16	Integrated Circuit, SN74164N 8-Bit Shift Register	TI	SN74164N	3
C10,C15,E10, E15	Integrated Circuit, SN7410ON 8-Bit Bistable Latch	TI	SN741ØØN	4
C11,C12,D11, D12,E11,E12, F11,F12,N13, N14,N15,N16	Integrated Circuit, SN74153N Dual 4-to-1 Line Multiplexer	TI	SN74153N	12
C16,E16,M5	Integrated Circuit, SN74165N 8-Bit Shift Register	TI	SN74165N	3
D7,H1	Integrated Circuit, SN7410N Triple 3-Input NAND Gate	TI	SN741ØN	2
D8,F8,F9, J3	Integrated Circuit, SN75154N Quad Line Receivers	TI	SN75154N	4
E1,J1,J4, L11	Integrated Circuit, N7411A Triple 3-Input AND Gate	SIG	N7411A	4
F6	Integrated Circuit, SN7437N Quad 2-Input NAND Buffer	TI	SN7437N	1
H4,J15,K15	Integrated Circuit, SN7442N 4-to-1 Line Decoder	TI	SN7442N	3

INTEGRATED CIRCUITS

REFERENCE	DESCRIPTION	PRIME MFR.	MFR. PART NO.	QTY.
H6,K13,L7, L9	Integrated Circuit, SN7420N Dual 4-Input NAND Gate	TI	SN742ØN	4
H8,J10	Integrated Circuit, SN75123N Dual Monostable Multivibrator	TI	SN74123N	2
H15,L14,M2	Integrated Circuit, N8202N 10-Bit Buffer Register	SIG	N82Ø2N	3
K9	Integrated Circuit, SN7454N 4-Wide, 2-Input AND-OR-Invert Gate	TI	SN7454N	1
L3	Integrated Circuit, SN7451N Dual 2-Wide, 2-Input AND-OR-Invert Gate	TI	SN7451N	1
L6	Integrated Circuit, SN74157N Quad 2-to-1 Line Multiplexer	TI	SN74157N	1
L15,M3,M13, M14,M15,N1, N2	Integrated Circuit, SN7486N Quad 2-Input Exclusive-OR Gate	TI	SN7486N	7
L16,M4	Integrated Circuit, SN7418ON 9-Bit Odd-Even Parity Generator	TI	SN7418ØN	2
M1	Integrated Circuit, US7429A Dual 4-Input NOR Gate	SPR	US7429A	1
N5,N7	Integrated Circuit Package 220/330Ω Resistance Network	BECK	899-5-R22Ø/33Ø	2
N9,N10	Integrated Circuit, SN7416N Hex Inverter Buffer/Driver	TI	SN7416N	2
N11,N12	Integrated Circuit, SN7417N Hex Buffer/Driver	TI	SN7417N	2
	Printed Circuit Board, Model 3120	BCP	92-ØØØ2258-1	1
	Connector, 40-Pin	MMM	3432-1ØØ2	2
	Bus Bar, 14.7 inches	BCP	25-Ø7Ø2114-3	2
	Bus Bar, 12.7 inches	BCP	25-Ø7Ø2115-2	5

12.5 IPS TAPE SPEED COMPONENTS

REFERENCE	DESCRIPTION	PRIME MFR.	MFR. PART NO.	QTY.
C35,C36	Capacitor, Mylar 0.033µF, 80 wvdc	SPR	192P3339R8	2
C41	Capacitor, Ceramic 0.1µF, 50 wvdc	AVX	CKØ5BX1Ø4K	1
R38	Resistor, Metal Film 28k, 1/8W, 1%	CGW	NA55-28Ø2F	1
R39	Resistor, Metal Film 37.4k, 1/8W, 1%	CGW	NA55-3742F	1
R47	Resistor, Metal Film 41.2k, 1/8W, 1%	CGW	NA55-4122F	1
Y1	Crystal, 4.2 MHZ	XTN	X-12-E 4.2 MHZ	1

15 IPS TAPE SPEED COMPONENTS

C35	Capacitor, Mylar 0.022µF, 80 wvdc	SPR	192P2239R8	1
C36	Capacitor, Mylar 0.01µF, 80 wvdc	SPR	192P1Ø39R8	1
C41	Capacitor, Mylar 0.047µF, 80 wvdc	SPR	192P4739R8	1
R38	Resistor, Metal Film 34k, 1/8W, 1%	CGW	NA55-34Ø2F	1
R39	Resistor, Metal Film 28k, 1/8W, 1%	CGW	NA55-28Ø2F	1
R47	Resistor, Metal Film 35.7k, 1/8W, 1%	CGW	NA55-3572F	1
Y1	Crystal, 4.2 MHZ	XTN	X-12-E 4.2 MHZ	

25 IPS TAPE SPEED COMPONENTS

C35	Capacitor, Mylar 0.022µF, 80 wvdc	SPR	192P2239R8	1
C36	Capacitor, Mylar 0.01µF, 80 wvdc	SPR	1921Ø39R8	1

REFERENCE	DESCRIPTION	PRIME MFR.	MFR. PART NO.	QTY.
C41	Capacitor, Mylar 0.047µF, 80 wvdc	SPR	192P4739R8	1
R38	Resistor, Metal Film 34k, 1/8W, 1%	CGW	NA55-34Ø2F	1
R39	Resistor, Metal Film 28k, 1/8W, 1%	CGW	NA55-28Ø2F	1
R47	Resistor, Metal Film 35.7k, 1/8W, 1%	CGW	NA55-3572F	1
Y1	Crystal, 4.2 MHZ	XTM	X-12-E 4.2 MHZ	
37.5 IPS TAPE SPEED COMPONENTS				
C35,36	Capacitor, Mylar 0.01µF, 80 wvdc	SPR	192P1Ø39R8	2
C41	Capacitor, Mylar 0.022µF, 80 wvdc	SPR	192P2239R8	1
R38	Resistor, Metal Film 28k, 1/8W, 1%	CGW	NA55-28Ø2F	
R39	Resistor, Metal Film 41.2k, 1/8W, 1%	CGW	NA55-4122F	1
R47	Resistor, Metal Film 49.9k, 1/8W, 1%	CGW	NA55-4992F	1
Y1	Crystal, 4.2 MHZ	XTN	X-12-E 4.2 MHZ	1
45 IPS TAPE SPEED COMPONENTS				
C35,36	Capacitor, Mylar 0.01µF, 80 wvdc	SPR	192P1Ø39R8	2
C41	Capacitor, Mylar 0.022µF, 80 wvdc	SPR	192P2239R8	1
R38	Resistor, Metal Film 23.2k, 1/8W, 1%	CGW	NA55-2322F	1
R39	Resistor, Metal Film 35.7k, 1/8W, 1%	CGW	NA55-3572F	1
R47	Resistor, Metal Film 41.2k, 1/8W, 1%	CGW	NA55-4122F	1

REFERENCE	DESCRIPTION	PRIME MFR.	MFR. PART NO.	QTY.
Y1	Crystal, 5.04 MHZ	XTN	X-12-E 5.Ø4 MHZ	1
75 IPS TAPE SPEED COMPONENTS				
C35,36	Capacitor, Mylar 0.01µF, 80 wvdc	SPR	192P1Ø39R8	2
C41	Capacitor, Mylar 0.022µF, 80 wvdc	SPR	192P2239R8	1
R38	Resistor, Metal Film 13.3k, 1/8W, 1%	CGW	NA55-1332F	1
R39	Resistor, Metal Film 20k, 1/8W, 1%	CGW	NA55-2ØØ2F	1
R47	Resistor, Metal Film 25.2k, 1/8W, 1%	CGW	NA55-2552F	1
Y1	Crystal, 4.2 MHZ	XTN	X-12-E 4.2 MHZ	1

SECTION 6

SCHEMATICS AND RELATED DRAWINGS

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LTR	DESCRIPTION	DATE	APP
A	DOCUMENTATION RELEASE E.O. 1253	2/11/75	DHE
B	ECO 212		

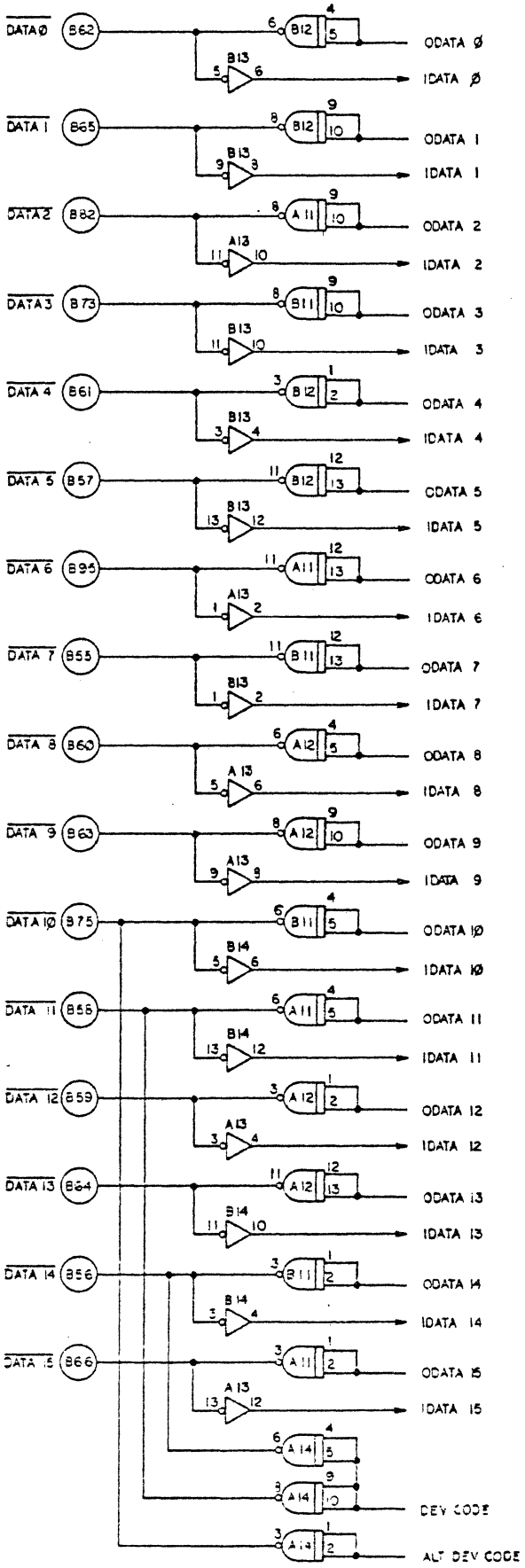
SHEET TITLE

2. SCHEMATIC INTERCONNECT
3. NOVA DATA TRANSCEIVERS / OUTPUT DRIVERS
4. NOVA CONTROL INPUT RECEIVERS
5. DEVICE SELECT LOGIC
6. COMMAND REGISTER / UNIT DECODE
7. COMMAND DECODE LOGIC
8. TAPE MOTION CONTROL
9. HIGH & LOW DENSITY CLOCKS
10. RAMP TIMING LOGIC
11. DIRECTION CHANGE LOGIC
12. BUSY / DONE LOGIC
13. INTERRUPT LOGIC
14. CHARACTER ASSEMBLY LOGIC 1
15. CHARACTER ASSEMBLY LOGIC 2
16. CHARACTER ASSEMBLY LOGIC 3
17. DATA CHANNEL LOGIC
18. MEMORY ADDRESS REGISTER
19. WORD COUNT REGISTER
20. WRITE STROBE GENERATOR
21. WRITE BUFFER
22. WRITE MUX / PARITY GENERATOR
23. LRC REGISTER
24. CRC REGISTER
25. TAPE OUTPUT DRIVERS
26. TAPE INPUT RECEIVERS
27. READ BUFFER
28. EOR DETECTION LOGIC
29. EOF / VERTICAL PARITY DETECTION LOGIC
30. STATUS REGISTER
31. DATA MULTIPLEXERS

DWG 96-0204214-1 B

96-0204252-5	UNIT 3120	Ball Computer Products, Inc. OAKLAND, CA 94618	
91-0204264-1	DRAWN LINDSTEDT	DATE 2/75	SCHEMATIC
	CHECK S SMITH	2/75	3120 TAPE CONTROLLER
	DESIGN		
	APP BY JEC	2-75	SIZE C DWG NO 96-0204214-1 REV B
REF. DOCUMENTATION	APP BY		SCALE RELEASE DATE 2-11-75 SH 1 /31

CURRENTLY UNAVAILABLE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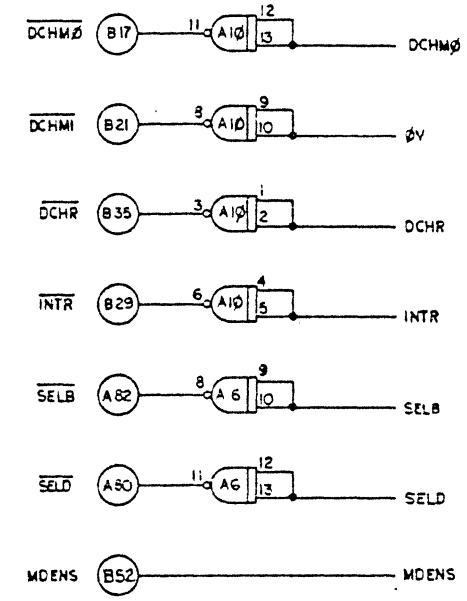
IDATA 15
DEV CODE
ALT DEV CODE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DCHMØ
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SELB A82
SELB
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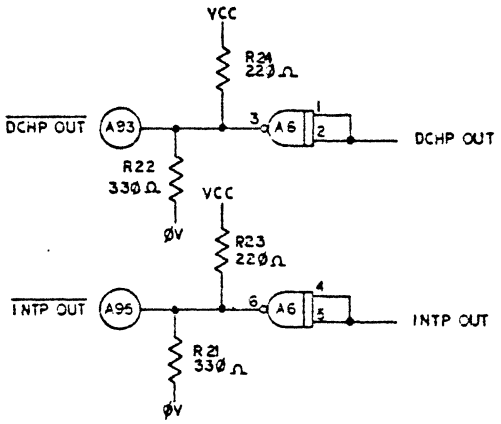
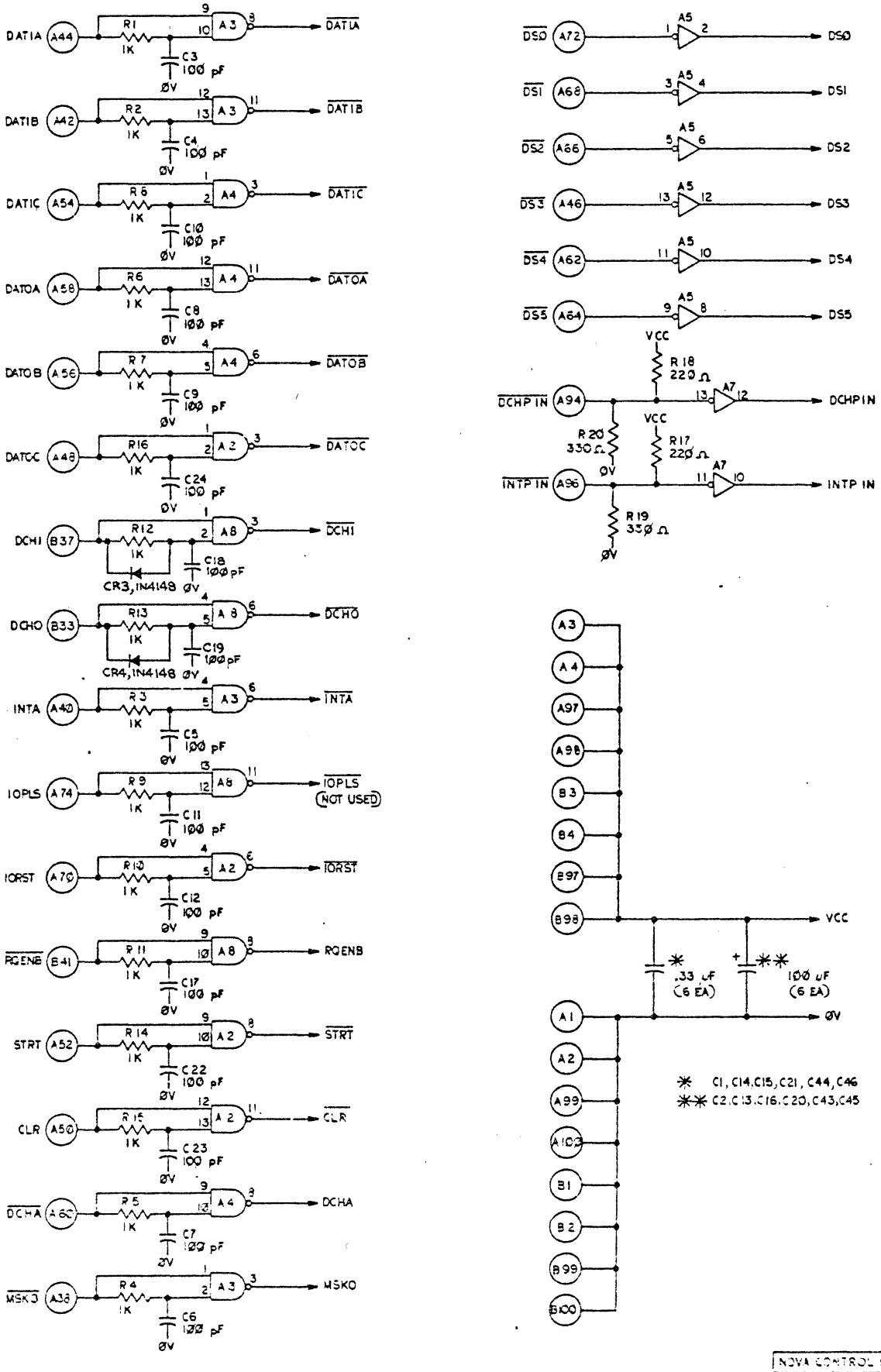
MDENS B52
MDENS


VCC
R24 220Ω
DCHP OUT A93
DCHP OUT
R22 330Ω
ØV
VCC
R23 220Ω
INTP OUT A95
INTP OUT
R21 330Ω
ØV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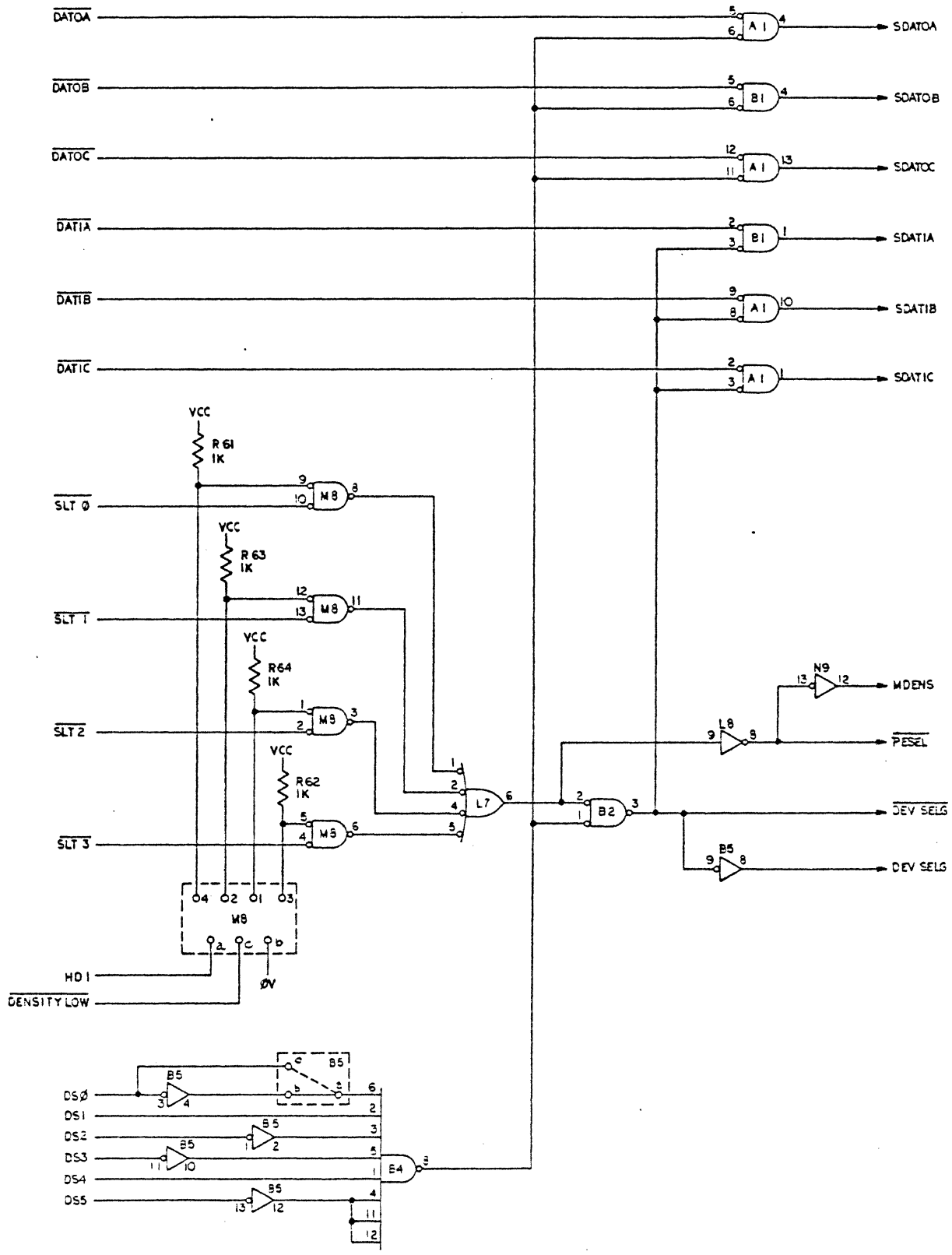
DATIB A42 R2 1K C4 100 pF ØV A3 DATIB
DATIC A54 R5 1K C10 100 pF ØV A4 DATIC
DATOA A58 R6 1K C8 100 pF ØV A4 DATOA
DATOB A56 R7 1K C9 100 pF ØV A4 DATOB
DATOC A48 R16 1K C24 100 pF ØV A2 DATOC
DCHI B37 R12 1K C18 100 pF ØV CR3, IN4148 A8 DCHI
DCHO B33 R13 1K C19 100 pF ØV CR4, IN4148 A8 DCHO
INTA A40 R3 1K C5 100 pF ØV A3 INTA
IOPLS A74 R9 1K C11 100 pF ØV A8 IOPLS (NOT USED)
IORST A70 R10 1K C12 100 pF ØV A2 IORST
RQENB B41 R11 1K C17 100 pF ØV A8 RQENB
STRT A52 R14 1K C22 100 pF ØV A2 STRT
CLR A50 R15 1K C23 100 pF ØV A2 CLR
DCHA A60 R5 1K C7 100 pF ØV A4 DCHA
MSKO A38 R4 1K C6 100 pF ØV A3 MSKO
DSØ A72 A5 DSØ
DSI A68 A5 DSI
DS2 A66 A5 DS2
DS3 A46 A5 DS3
DS4 A62 A5 DS4
DS5 A64 A5 DS5
VCC
R18 220 Ω
DCHPIN A94 A7 DCHPIN
R20 330 Ω ØV
VCC
R17 220 Ω
INTPIN A96 A7 INTP IN
R19 33Ø Ω ØV
A3
A4
A97
A98
B3
B4
B97
B98 VCC
.33 uF (6 EA)
100 uF (6 EA)
A1 ØV
A2
A99
A100
B1
B2
B99
B100
* C1, C14, C15, C21, C44, C46
** C2, C13, C16, C20, C43, C45



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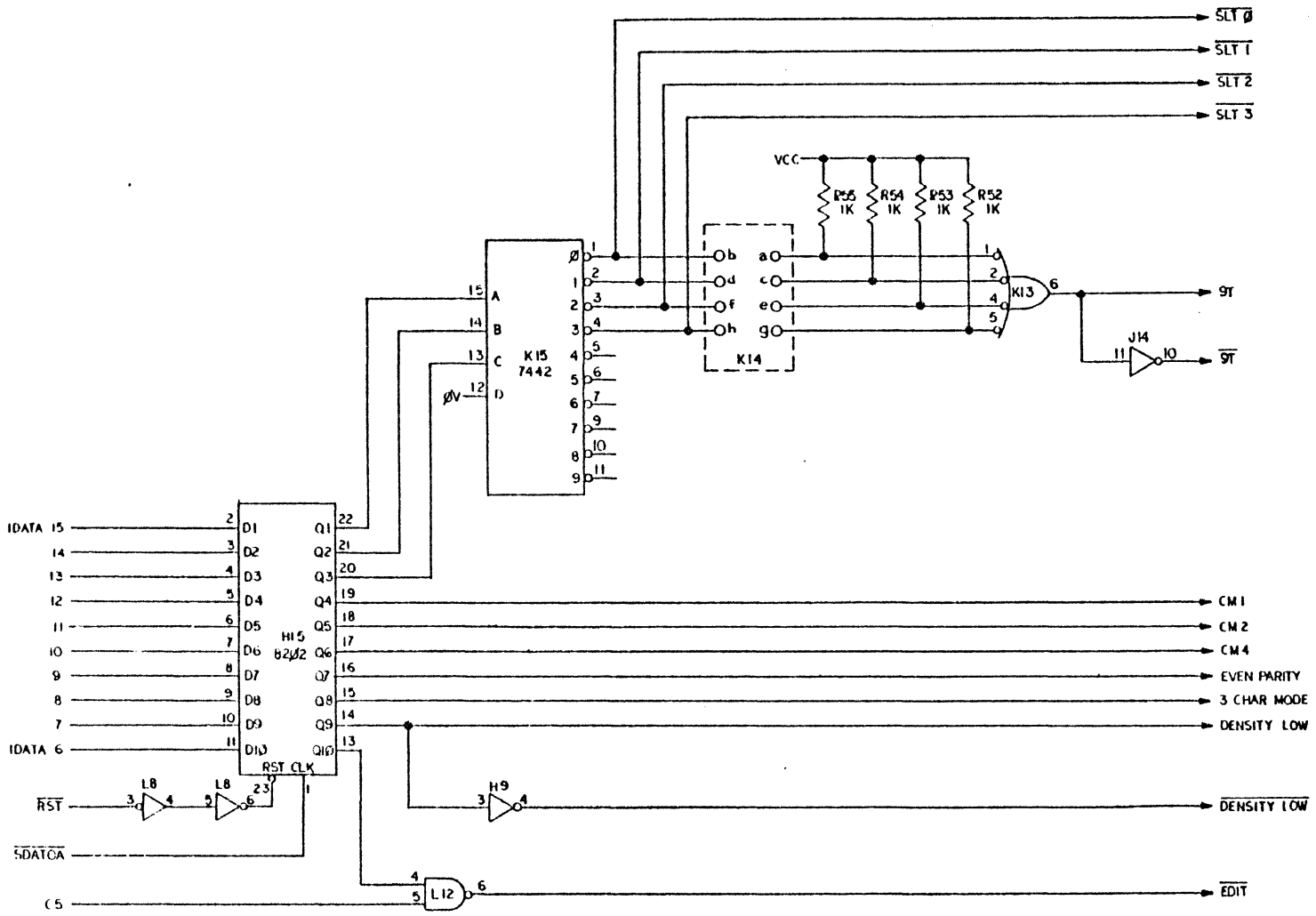

COMMAND REGISTER/UNIT DECODE

96-0200421-1

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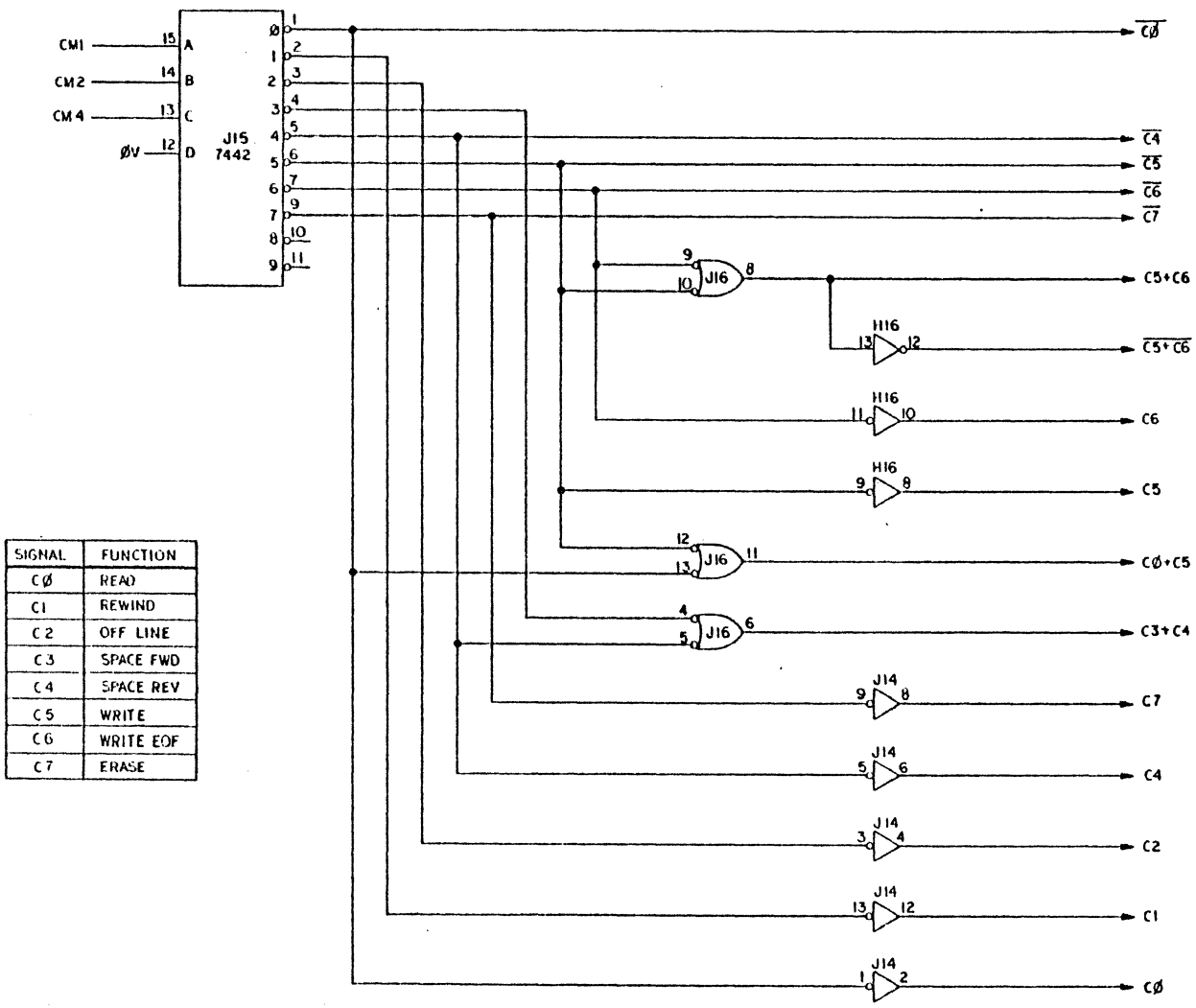

SIGNAL	FUNCTION
CØ	READ
C1	REWIND
C2	OFF LINE
C3	SPACE FWD
C4	SPACE REV
C5	WRITE
C6	WRITE EOF
C7	ERASE

COMMAND DECODE LOGIC

96-02-42141

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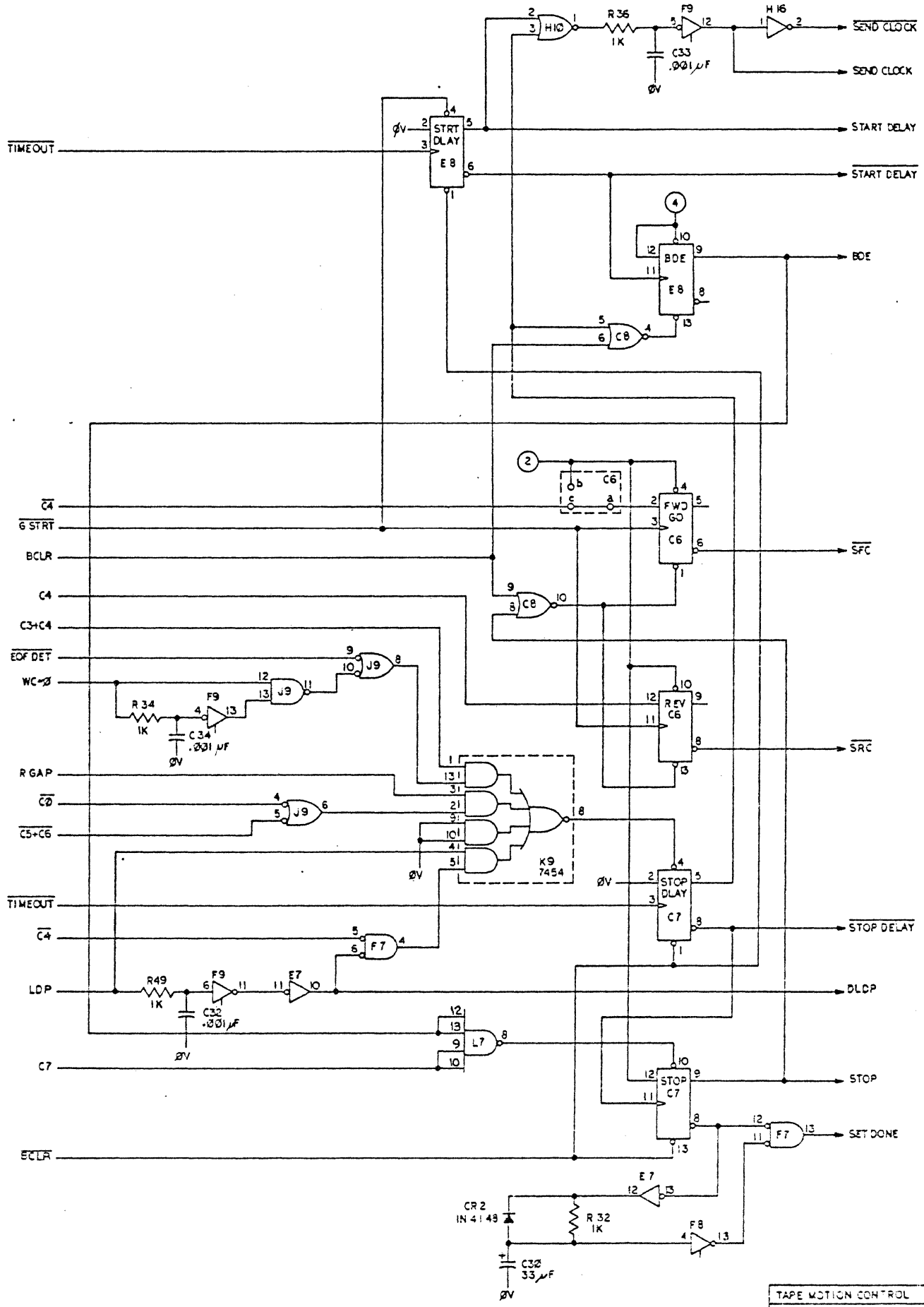
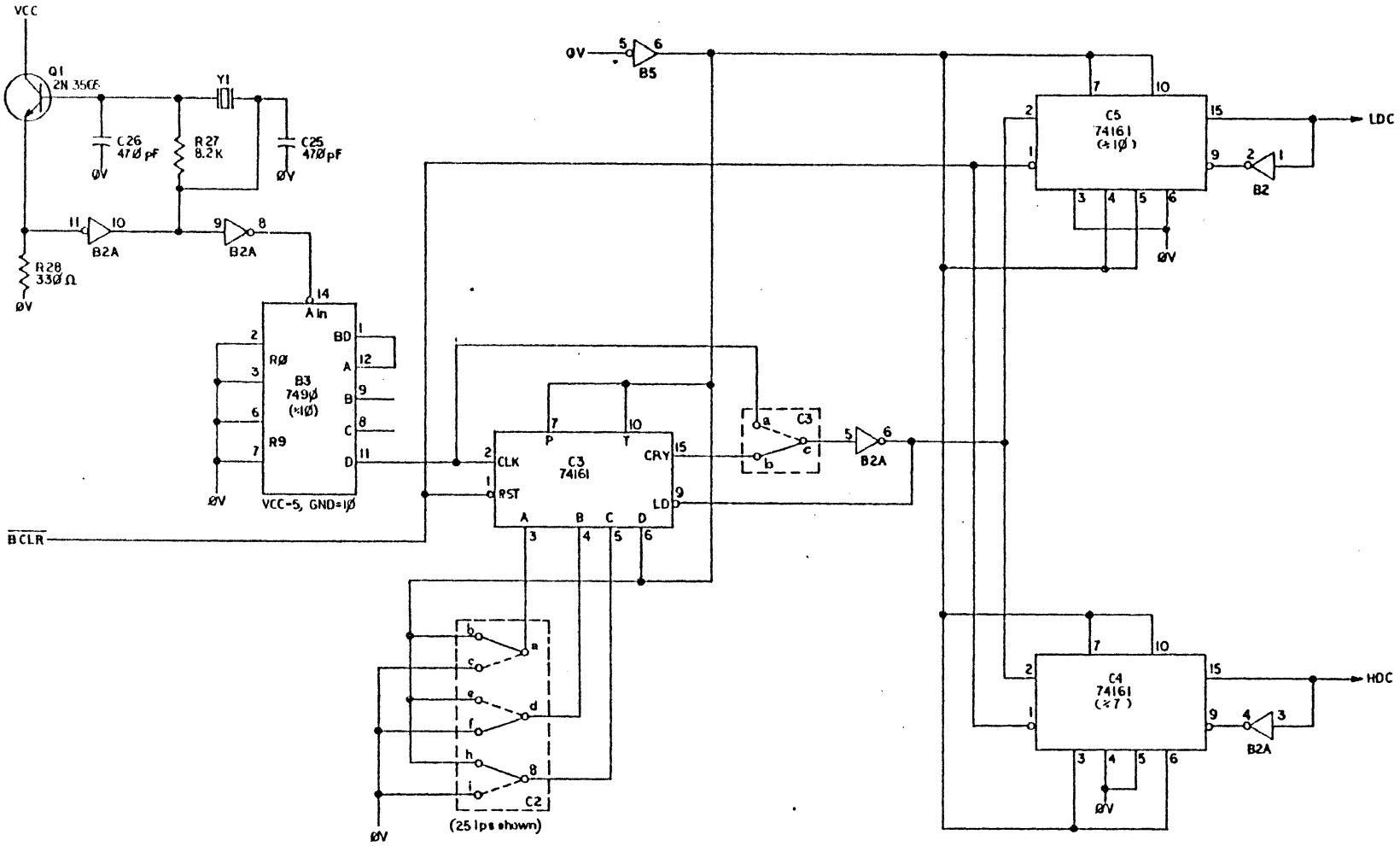
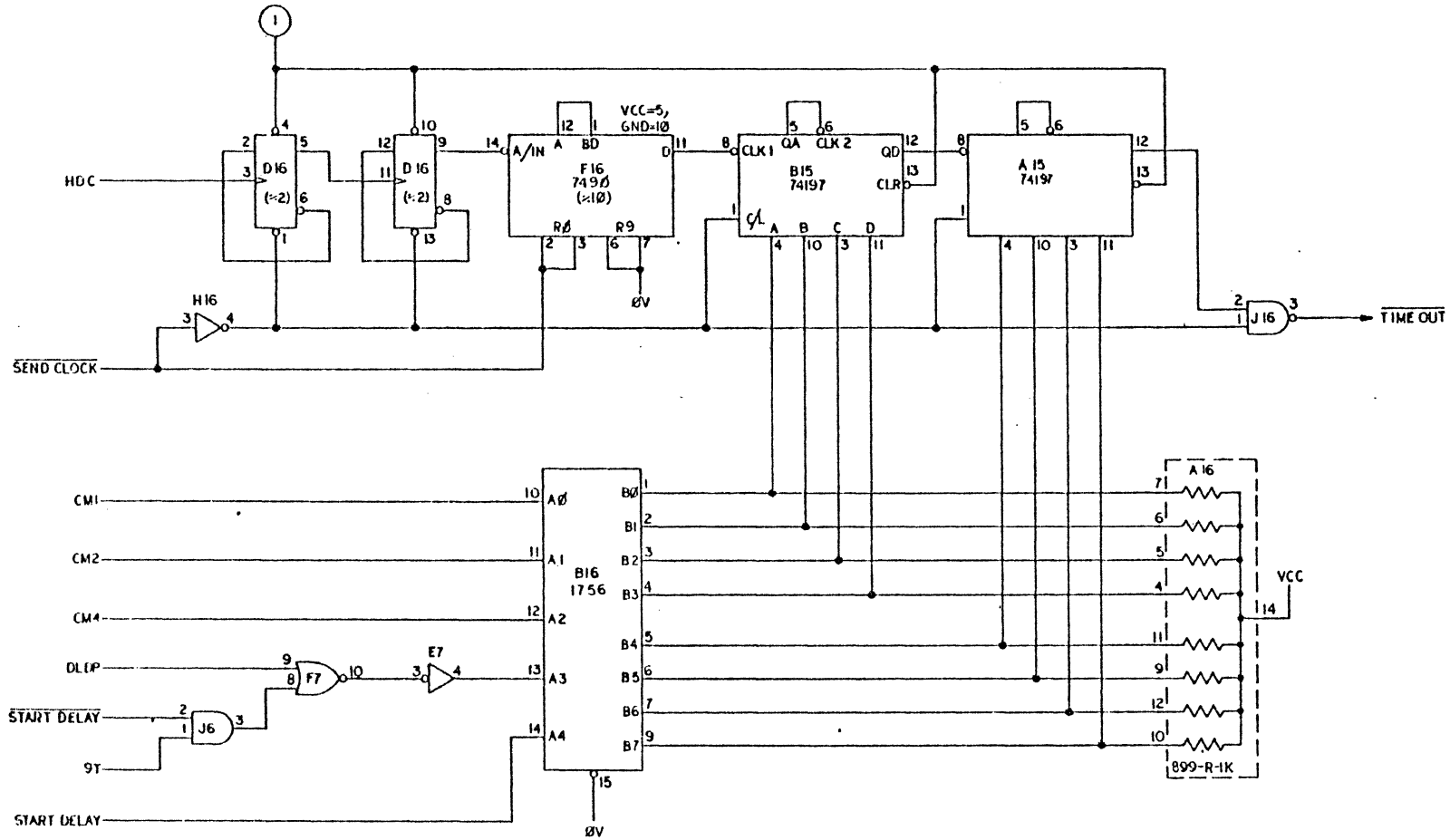


TAPE MOTION CONTROL	
98-02042-4-1	8 OF 31


VCC
Q1
2N 3568
Y1
C26
470 pF
R27
8.2K
C25
470 pF
ØV
R28
330Ω
B2A
B2A
A In
B3
749Ø
(÷10)
VCC-5, GND=Ø
BCLR
C3
74161
CLK
RST
CRY
LD
P
T
A
B
C
D
C3
B2A
B5
C5
74161
(÷10)
LDC
B2
C4
74161
(÷7)
HDC
B2A
C2
(25 lps shown)



RAMP TIMING LOGIC

96-220421A-1

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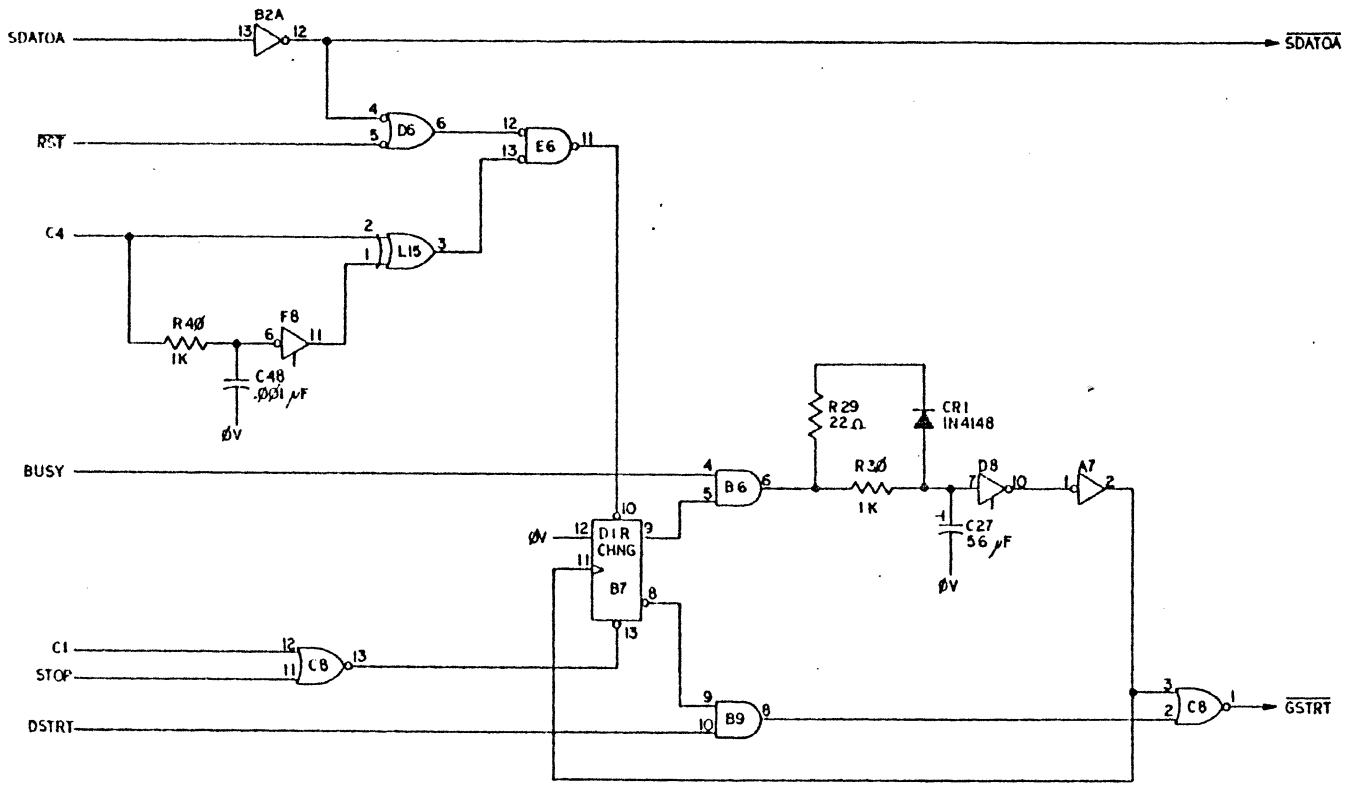
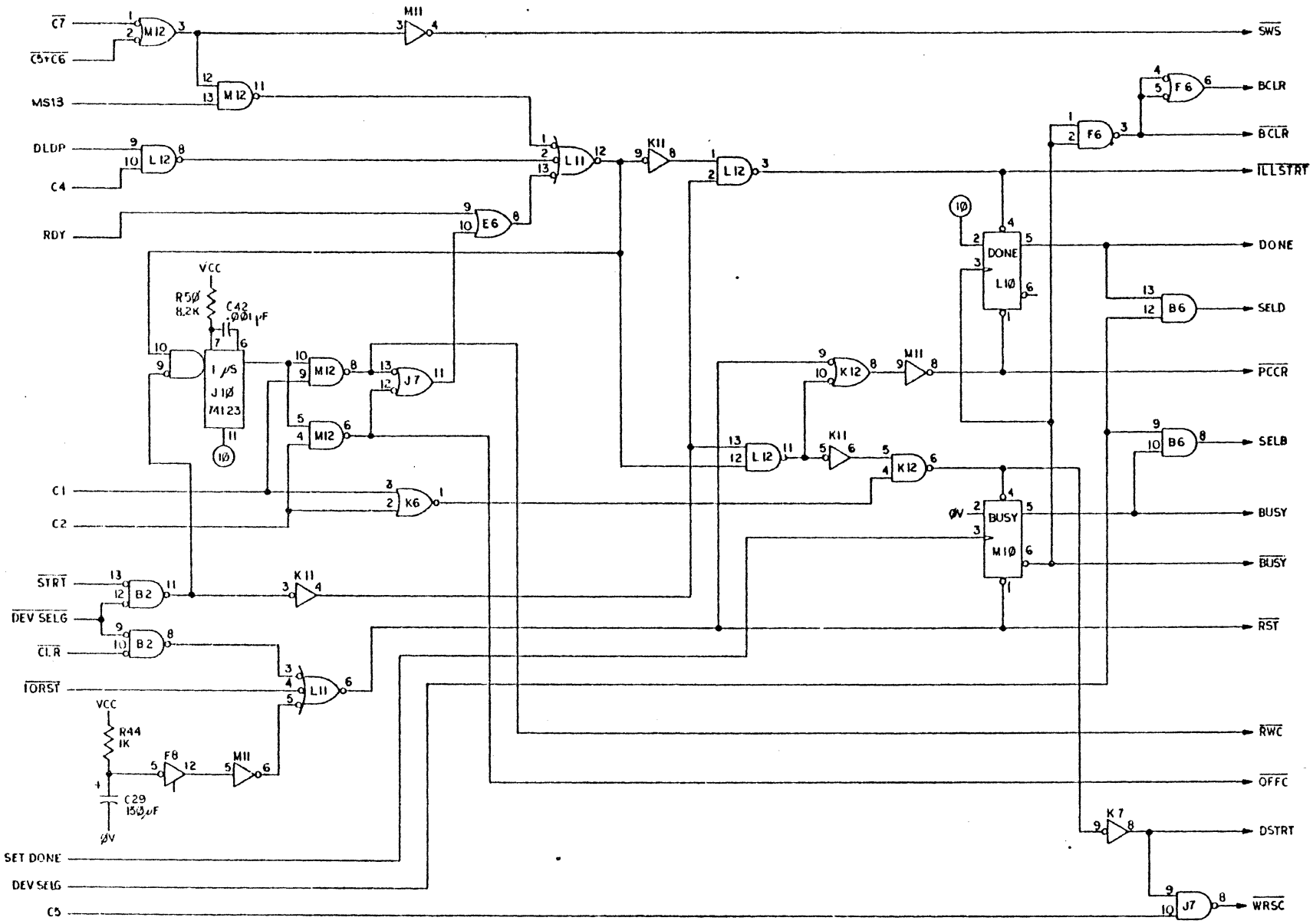
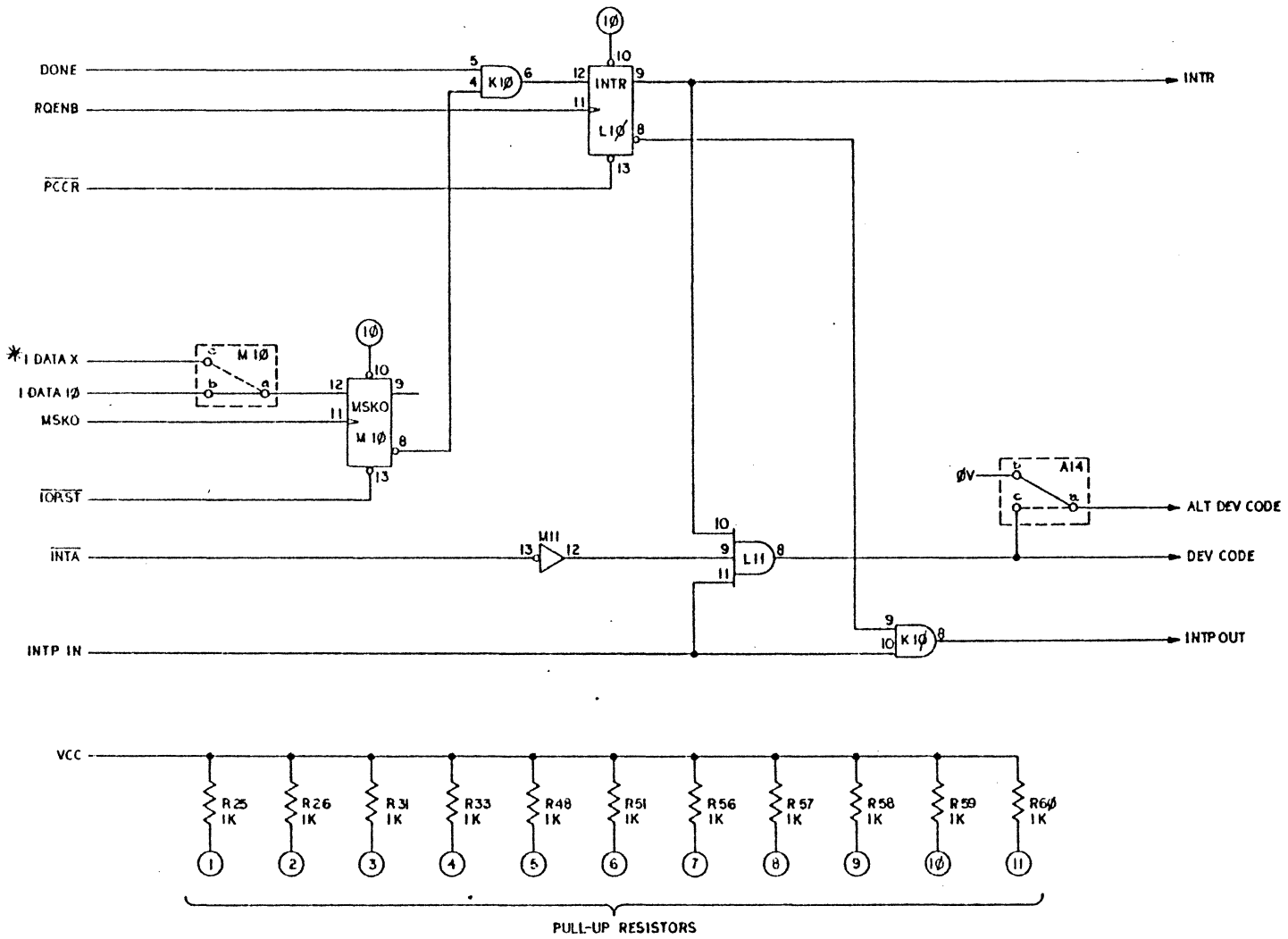
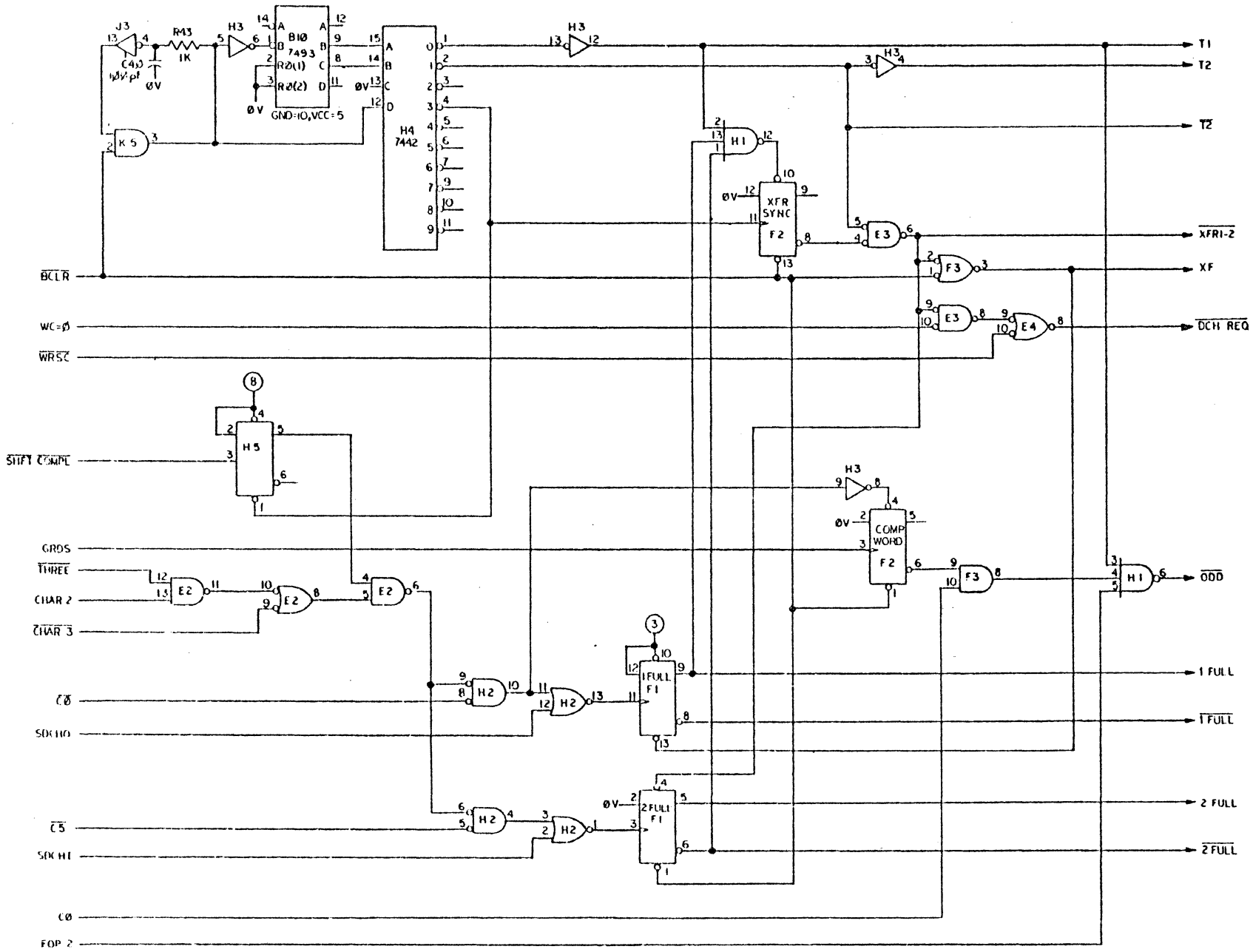

SDATOA
B2A
SDATOA
RST
D6
E6
C4
L15
R4Ø
1K
F8
C48
.ØØ1 µF
ØV
R29
22Ω
CR1
IN4148
BUSY
B6
R3Ø
1K
D8
A7
C27
56 µF
ØV
ØV
DIR
CHNG
B7
C1
STOP
C8
DSTRT
B9
C8
GSTRT


C7
C5+C6
MS13
DLDP
C4
RDY
VCC
R50
8.2K
C42
.0001 µF
1 µS
J10
M123
C1
C2
STRT
DEV SELG
CLR
IORST
VCC
R44
1K
C29
150 µF
ØV
SET DONE
DEV SELG
C5
SWS
BCLR
BCLR
ILLSTRT
DONE
SELD
PCCR
SELB
BUSY
BUSY
RST
RWC
OFFC
DSTRT
WRSC
DONE
L10
BUSY
M10



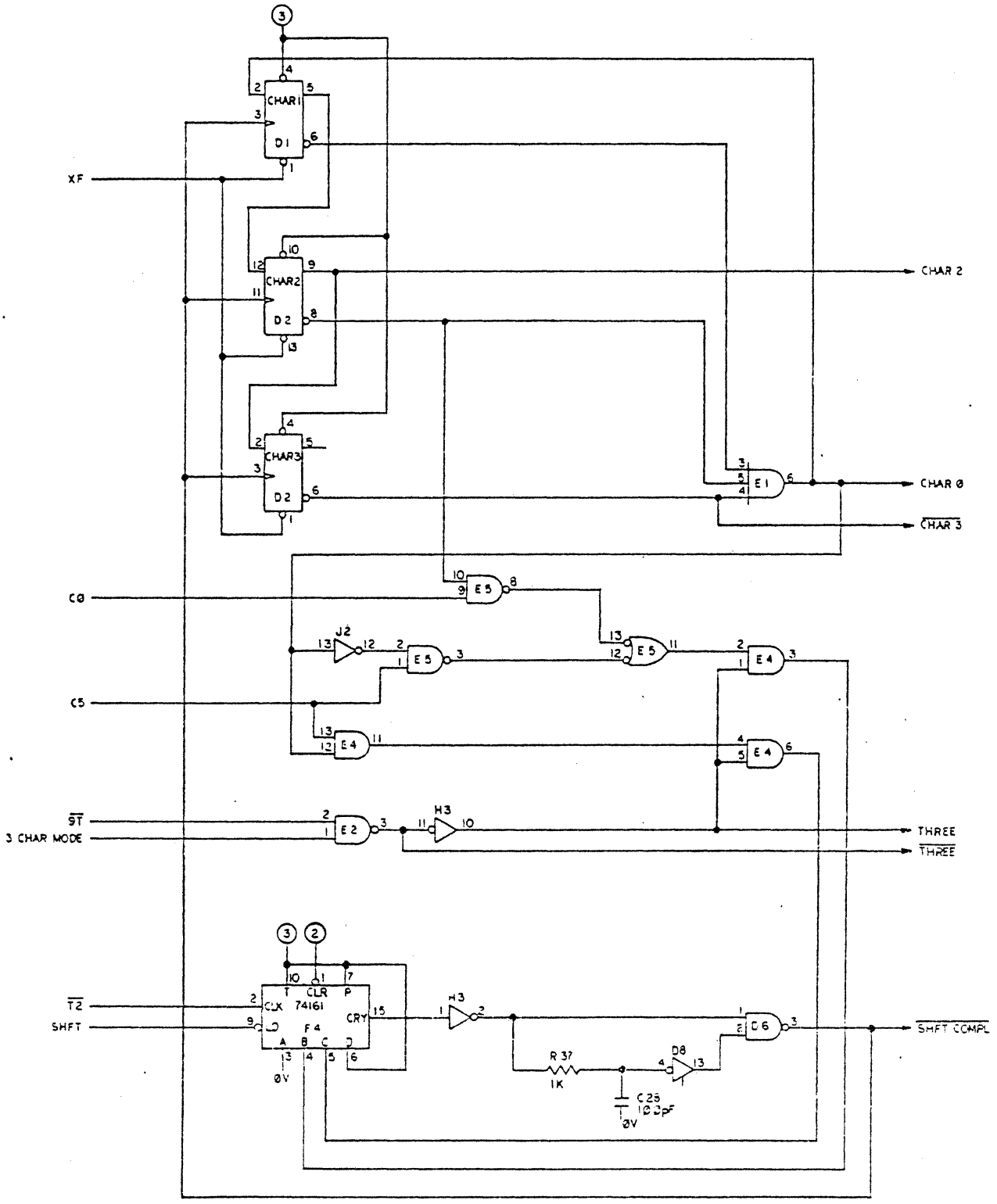
* I DATA X MUST BE HARDWIRED



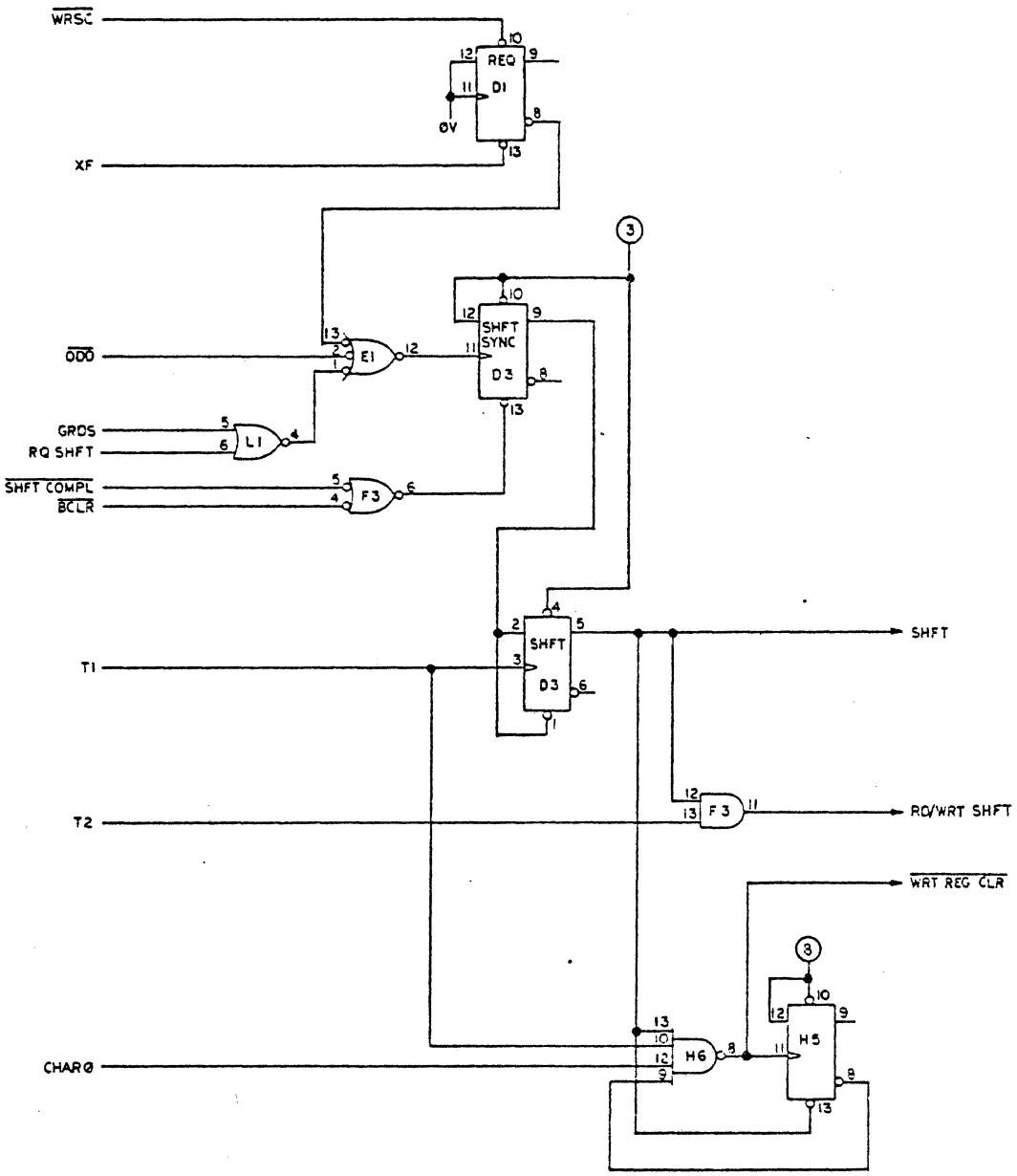
CHARACTER ASSEMBLY LOGIC 1

PMS-2204214-1

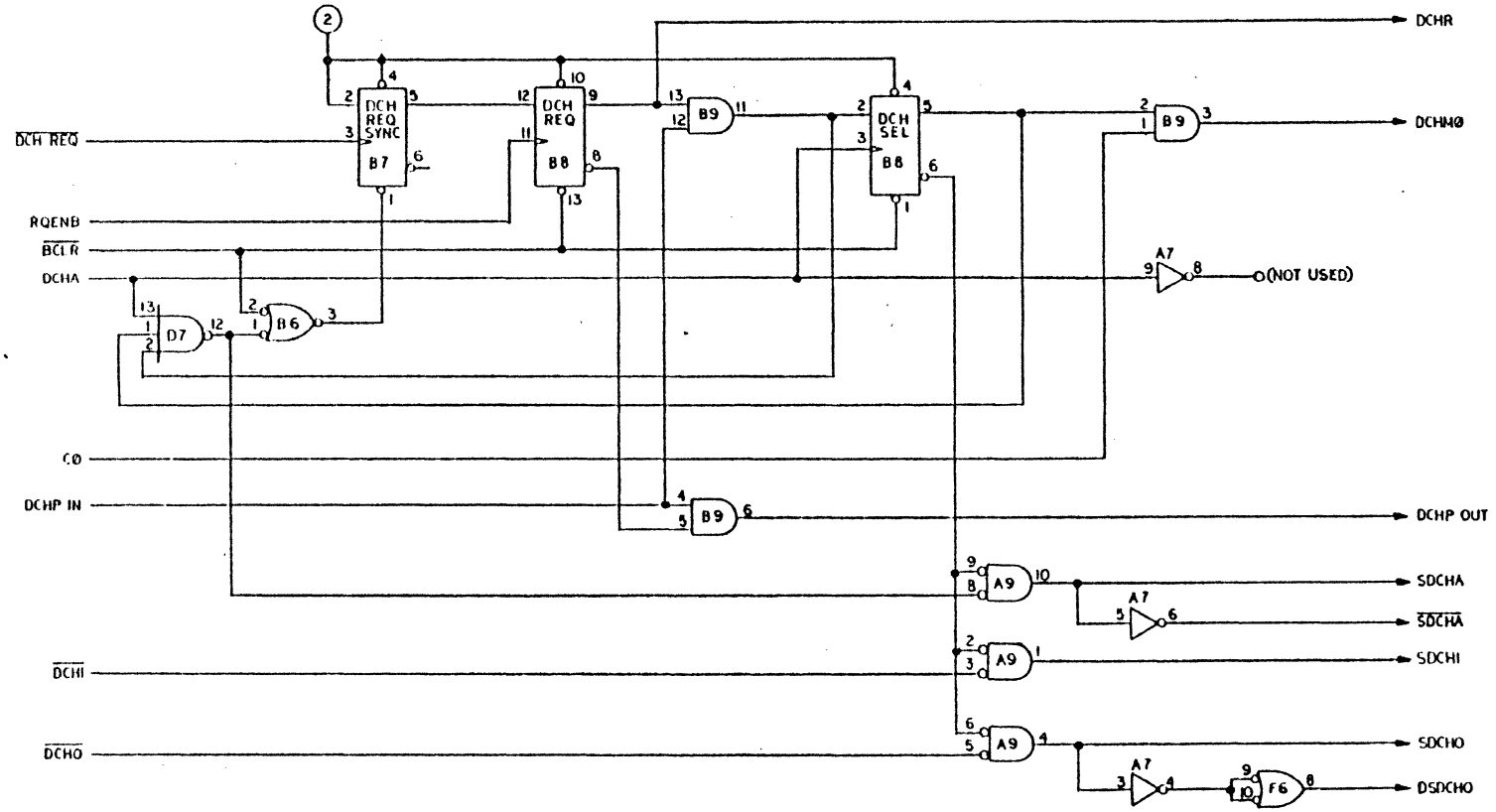
14 OF 31

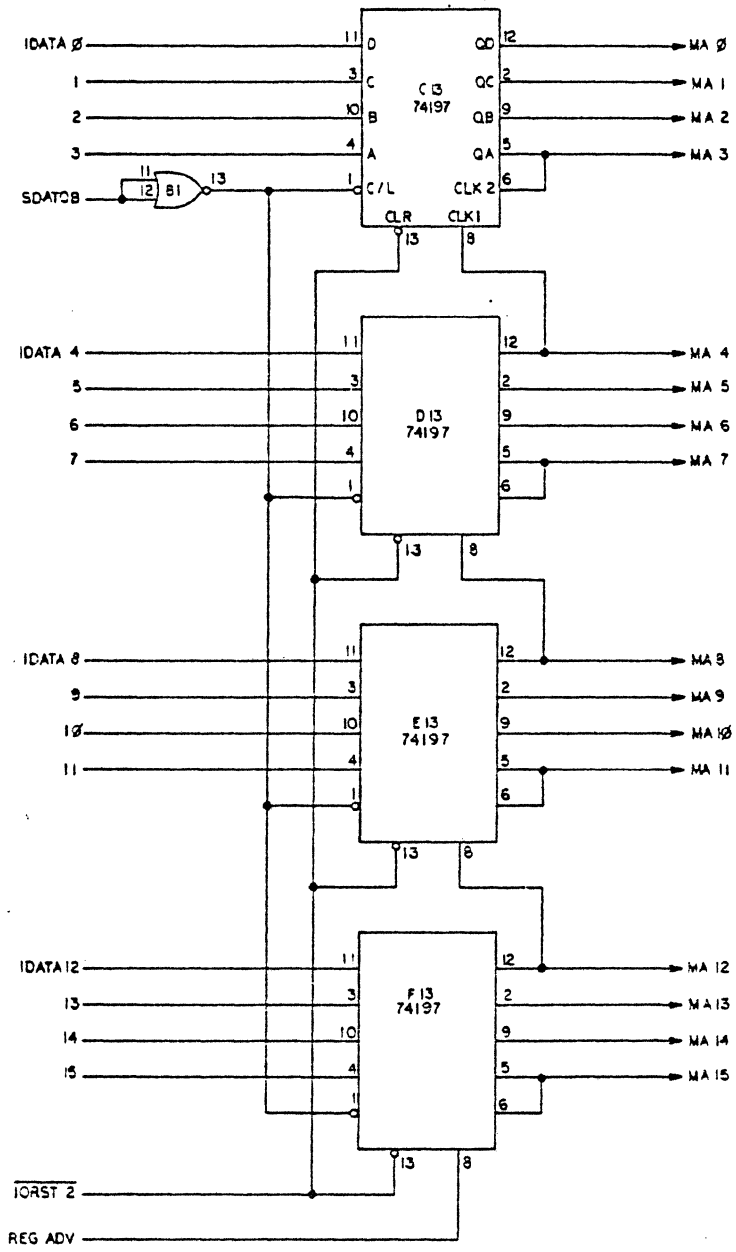


CHARACTER ASSEMBLY LOGIC 2	
96-002042H4-1	15 OF 31

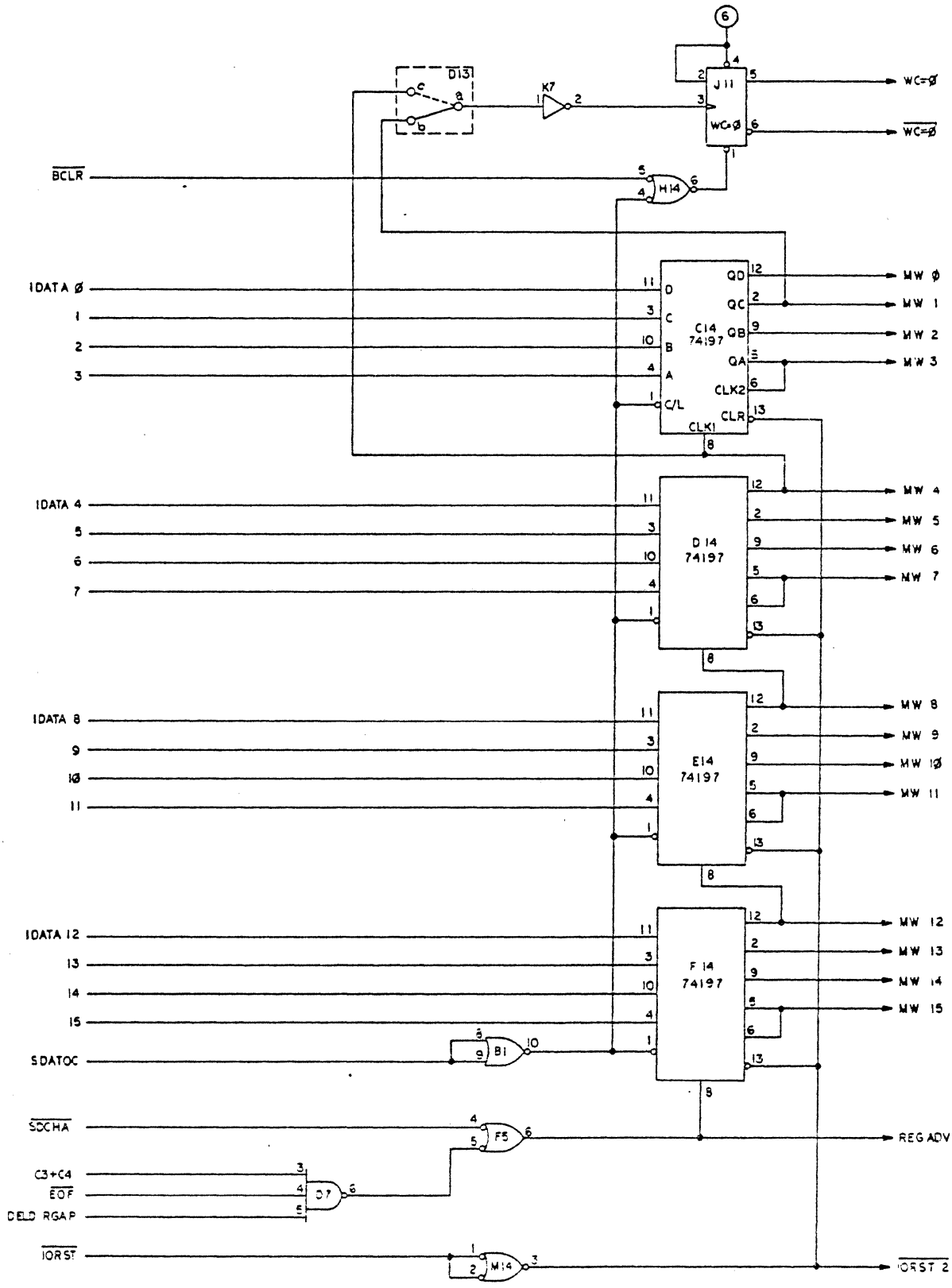


CHARACTER ASSEMBLY LOGIC 3	
96-0204214-1	16 OF 31

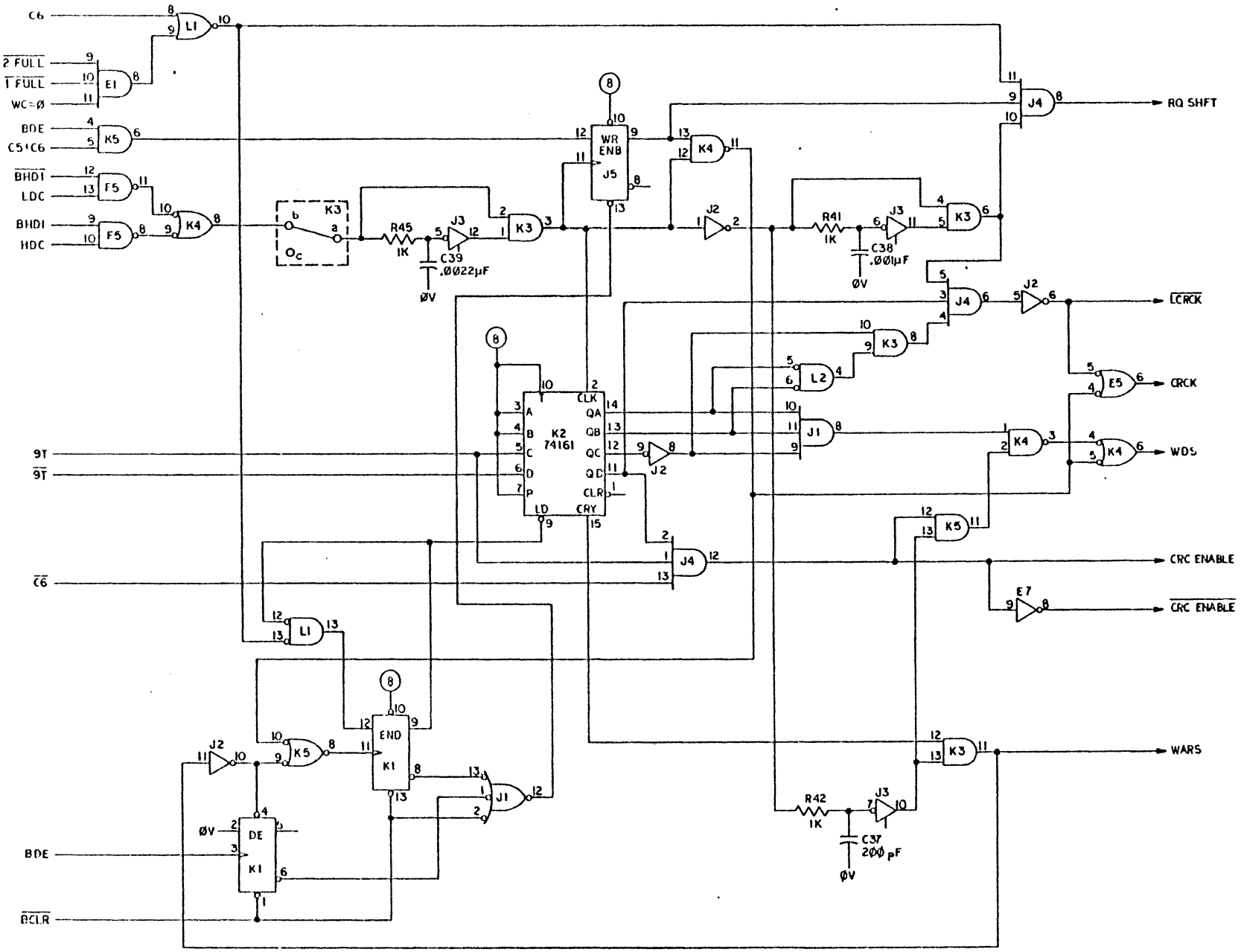

2
DCH REQ
RQENB
BCLR
DCHA
CO
DCHP IN
DCHI
DCHO
DCH REQ SYNC
B7
DCH REQ
B8
DCH SEL
B8
B9
B9
B9
B6
D7
A7
A7
A7
A9
A9
A9
F6
DCHR
DCHM0
(NOT USED)
DCHP OUT
SDCHA
SDCHA
SDCHI
SDCHO
DSDCHO



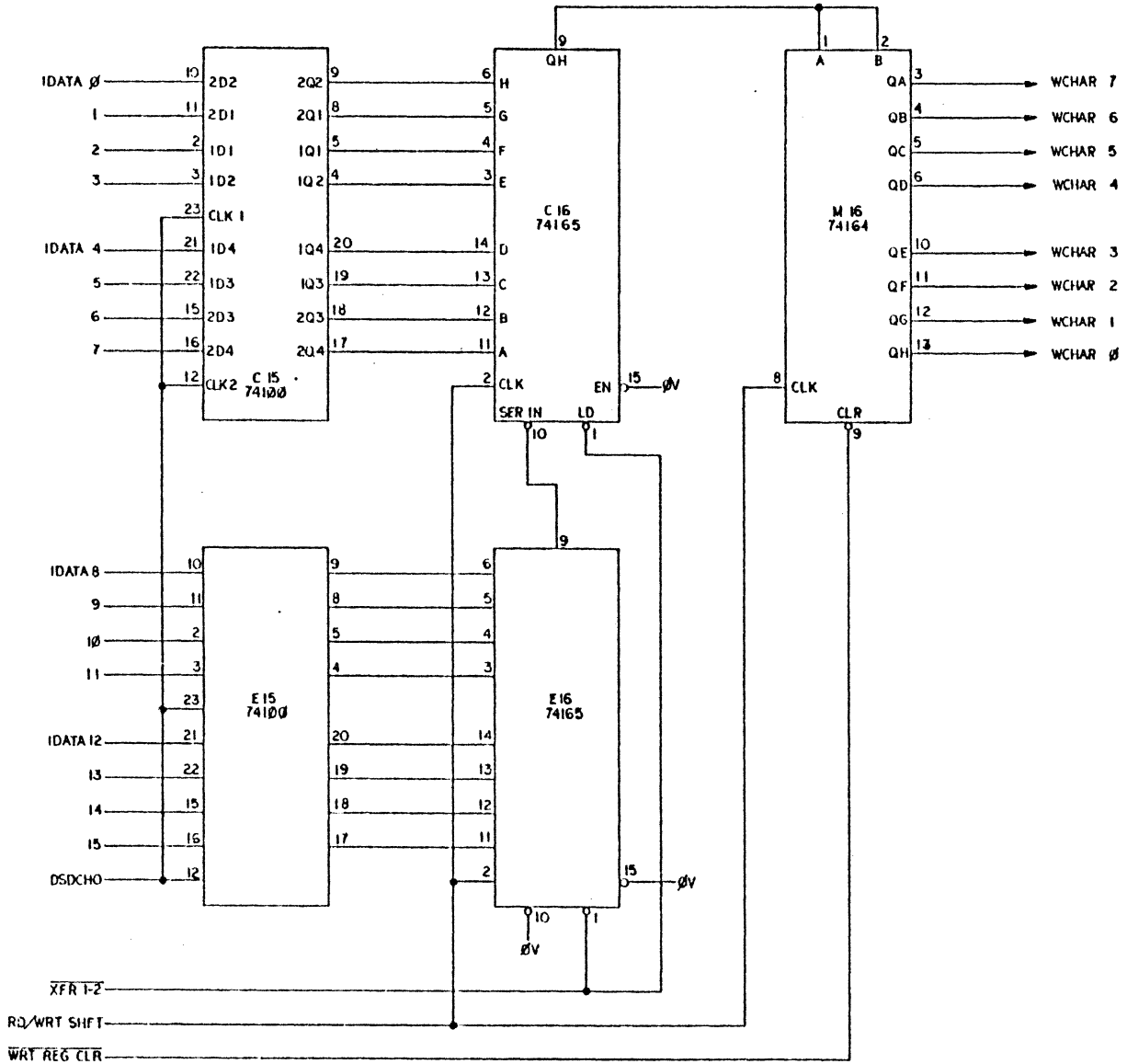
MEMORY ADDRESS REGISTER	
36-0204214-1	18 OF 31

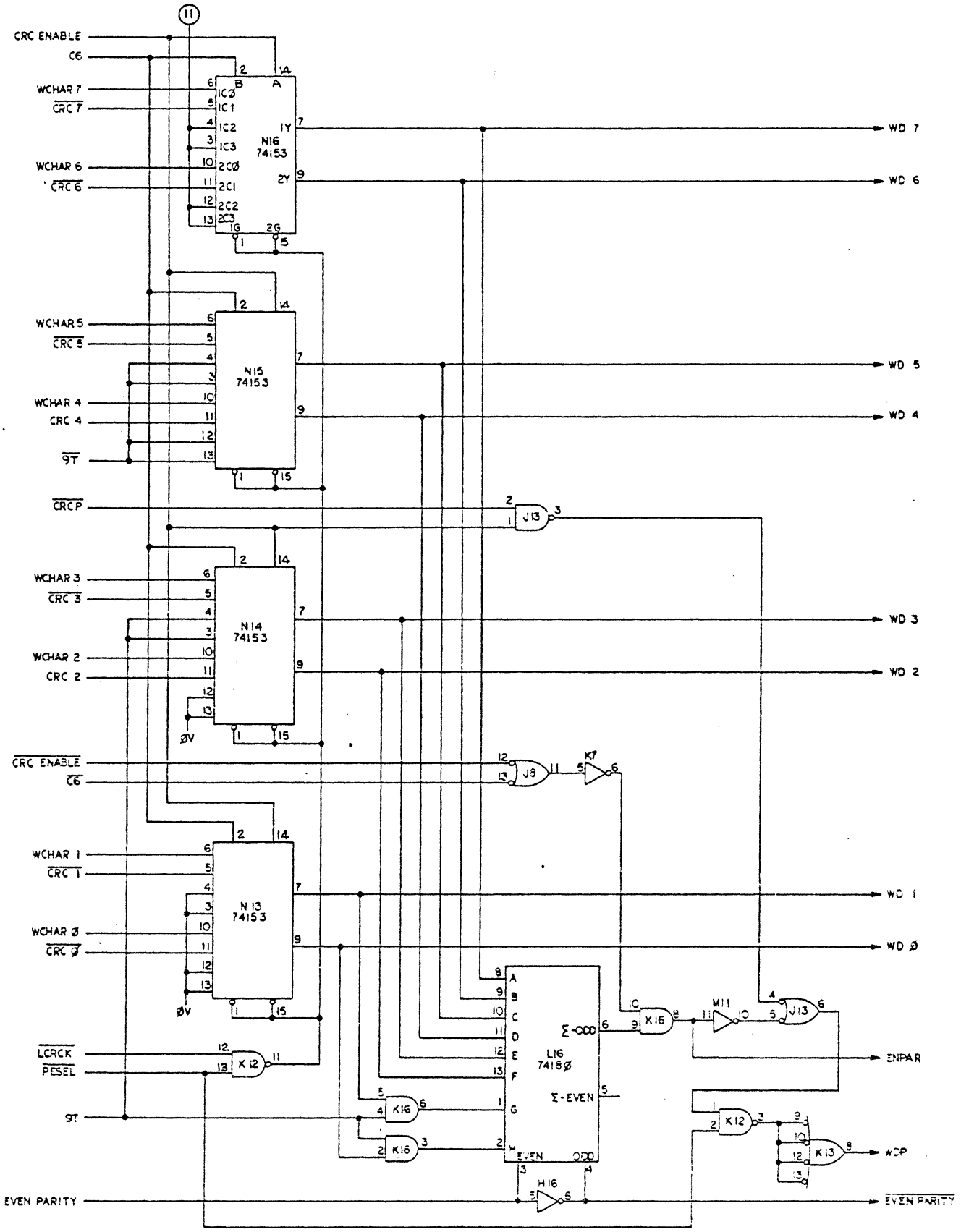


WORD COUNT REGISTER	
96-0304214-1	19 OF 31



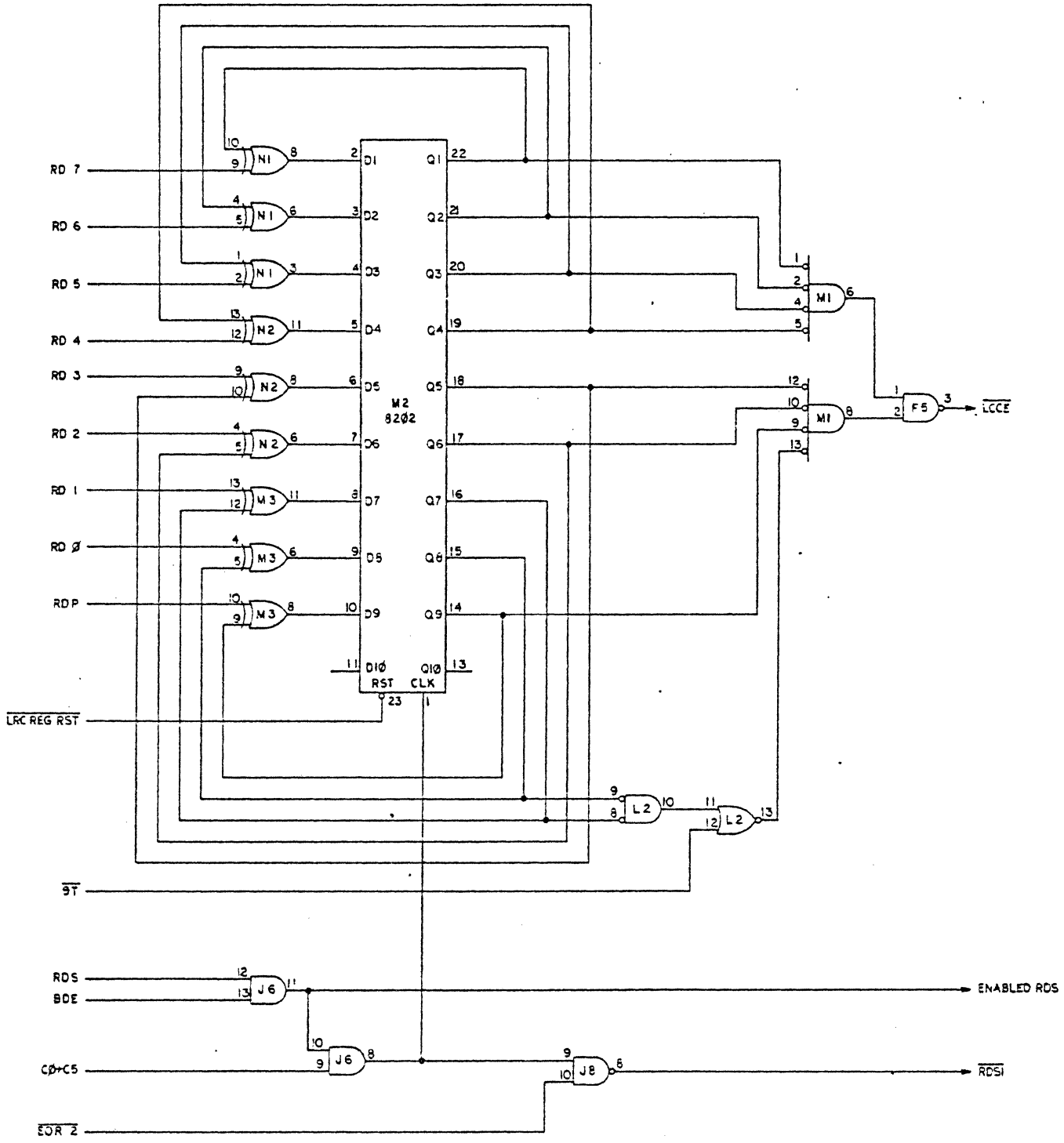
WRITE STROBE GENERATOR
96-00234-1
20 OF 31


IDATA Ø
1
2
3
IDATA 4
5
6
7
2D2
2D1
1D1
1D2
CLK 1
1D4
1D3
2D3
2D4
CLK2
C 15
74100
2Q2
2Q1
1Q1
1Q2
1Q4
1Q3
2Q3
2Q4
C 16
74165
QH
H
G
F
E
D
C
B
A
CLK
EN
SER IN
LD
ØV
M 16
74164
A
B
QA
QB
QC
QD
QE
QF
QG
QH
CLK
CLR
WCHAR 7
WCHAR 6
WCHAR 5
WCHAR 4
WCHAR 3
WCHAR 2
WCHAR 1
WCHAR Ø
IDATA 8
9
10
11
IDATA 12
13
14
15
DSDCH0
E 15
74100
E 16
74165
XFR 1-2
RD/WRT SHFT
WRT REG CLR

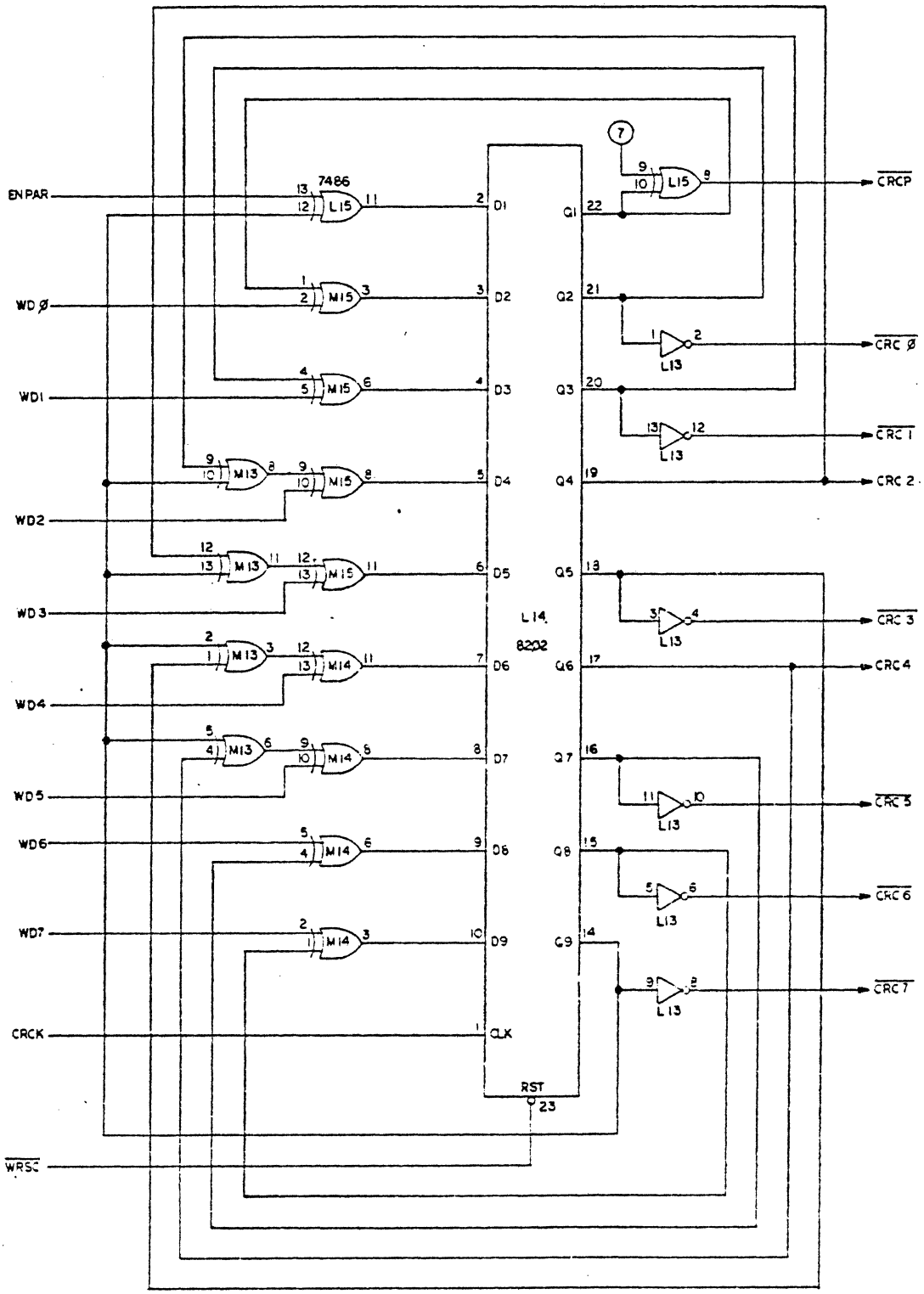


WRITE MUX / PARITY GENERATOR

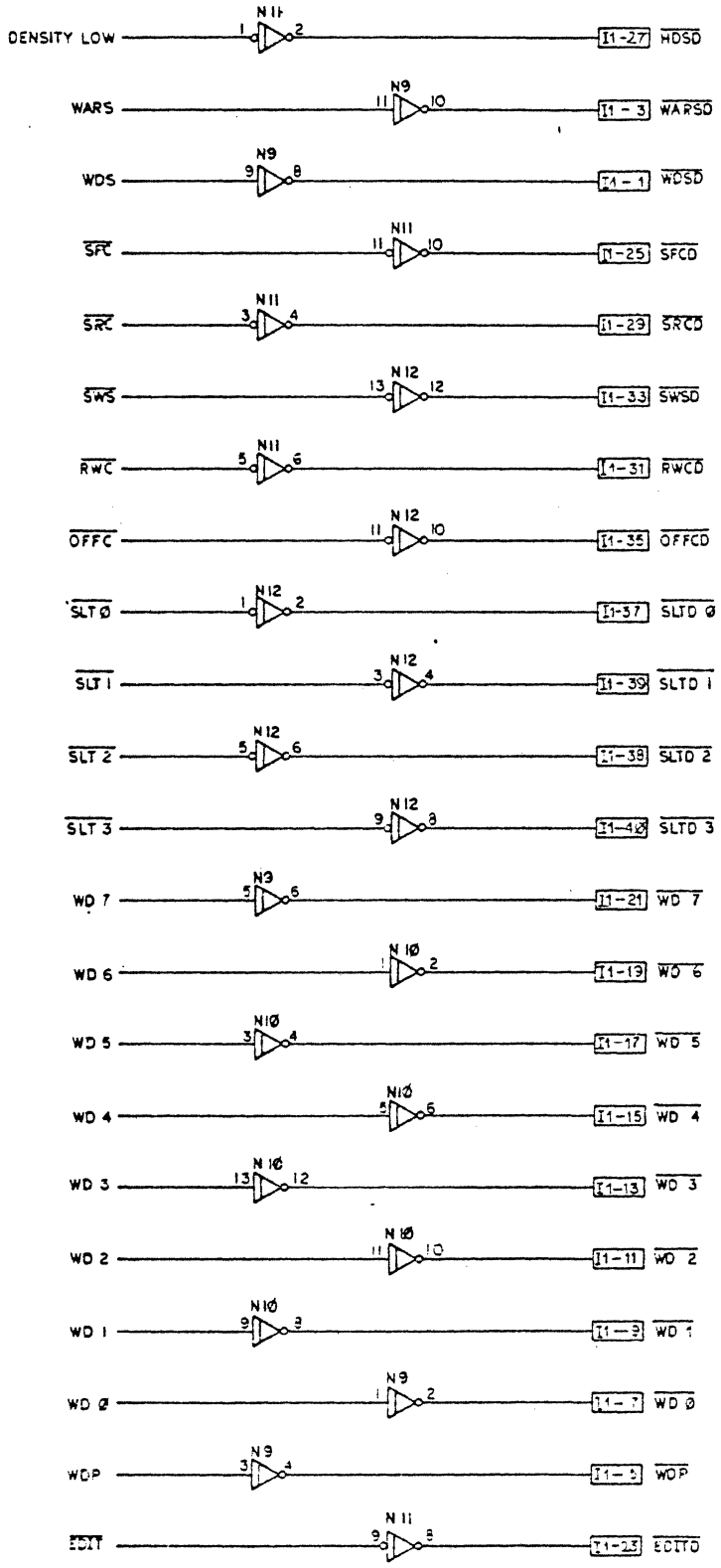
96-02C421A-1 22 OF 31



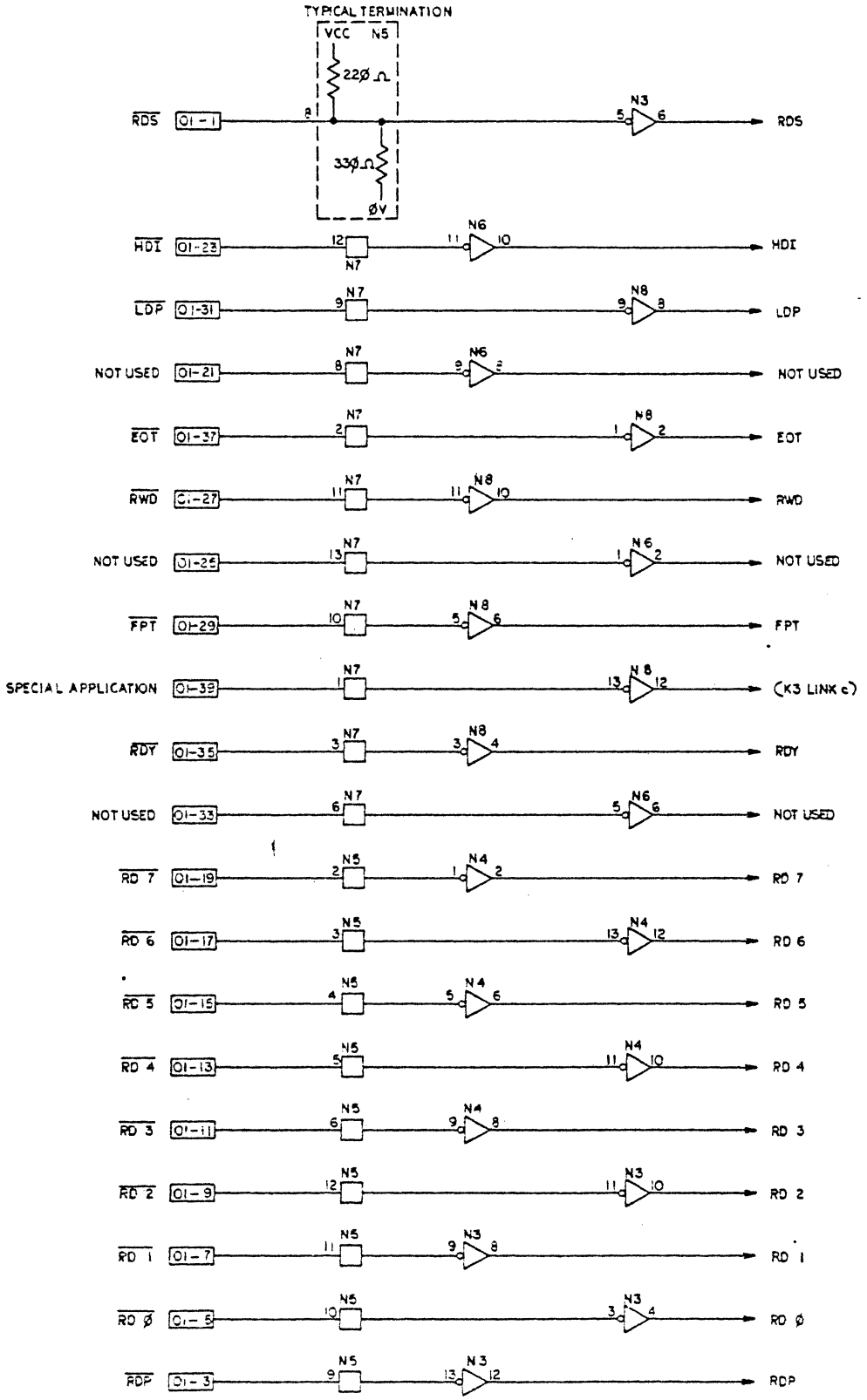
LRC REGISTER	
68-0204214-1	3.3 OF 3.4



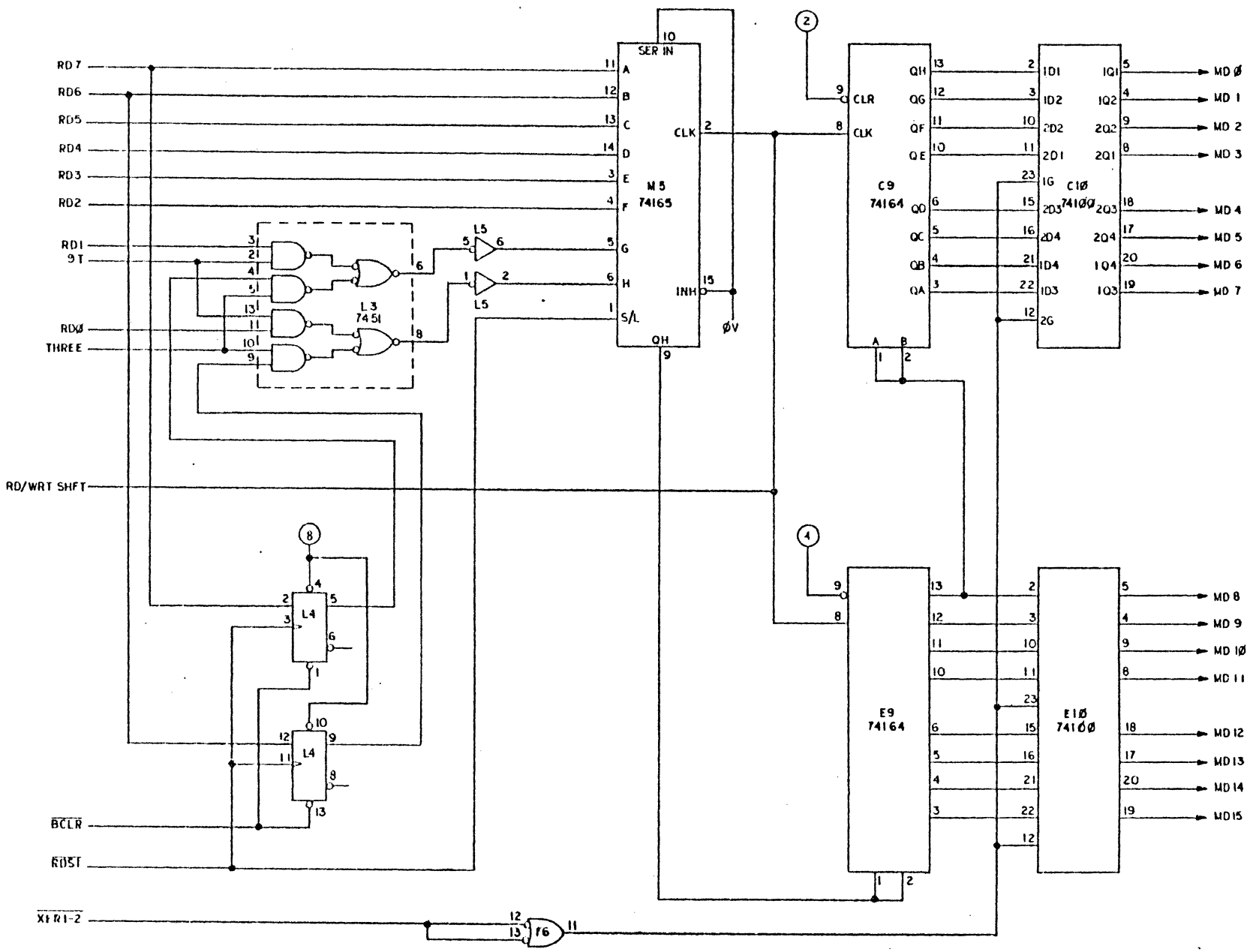
CRC REGISTER	
96-02042A-1	24 OF 31

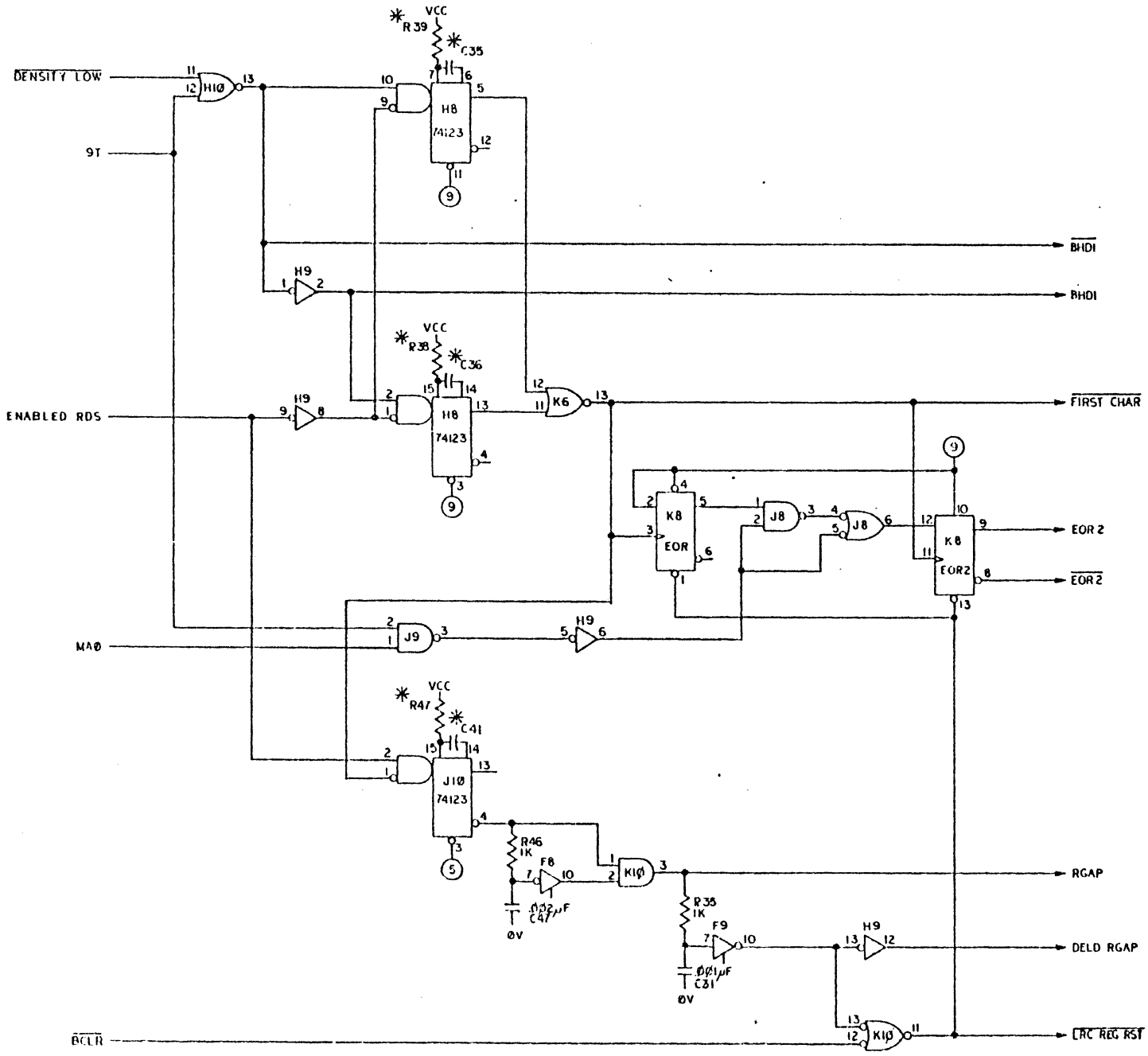


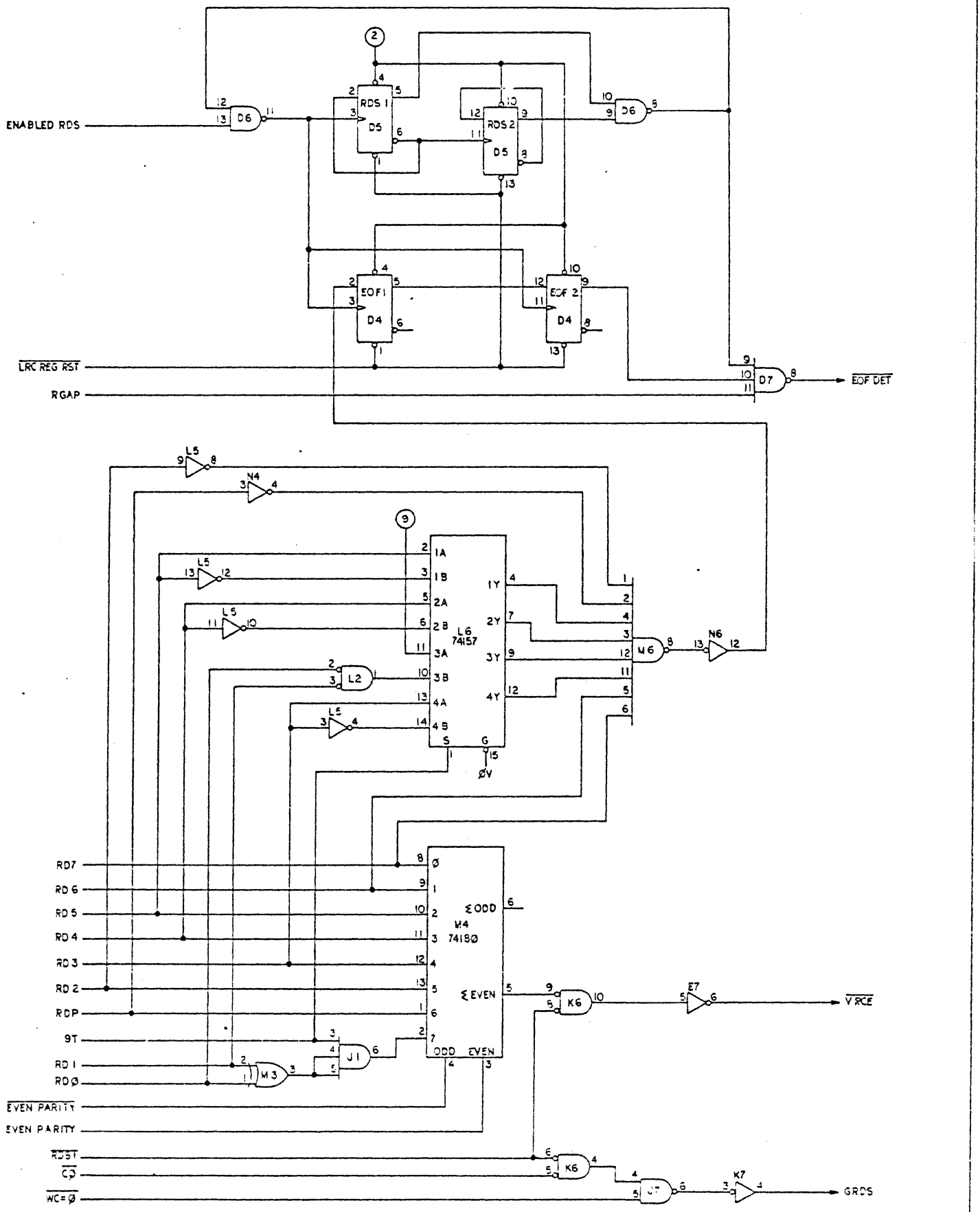
EVEN NUMBERED PINS 2-36 (INCLUSIVE) ARE SIGNAL RETURN GROUND (ØV)



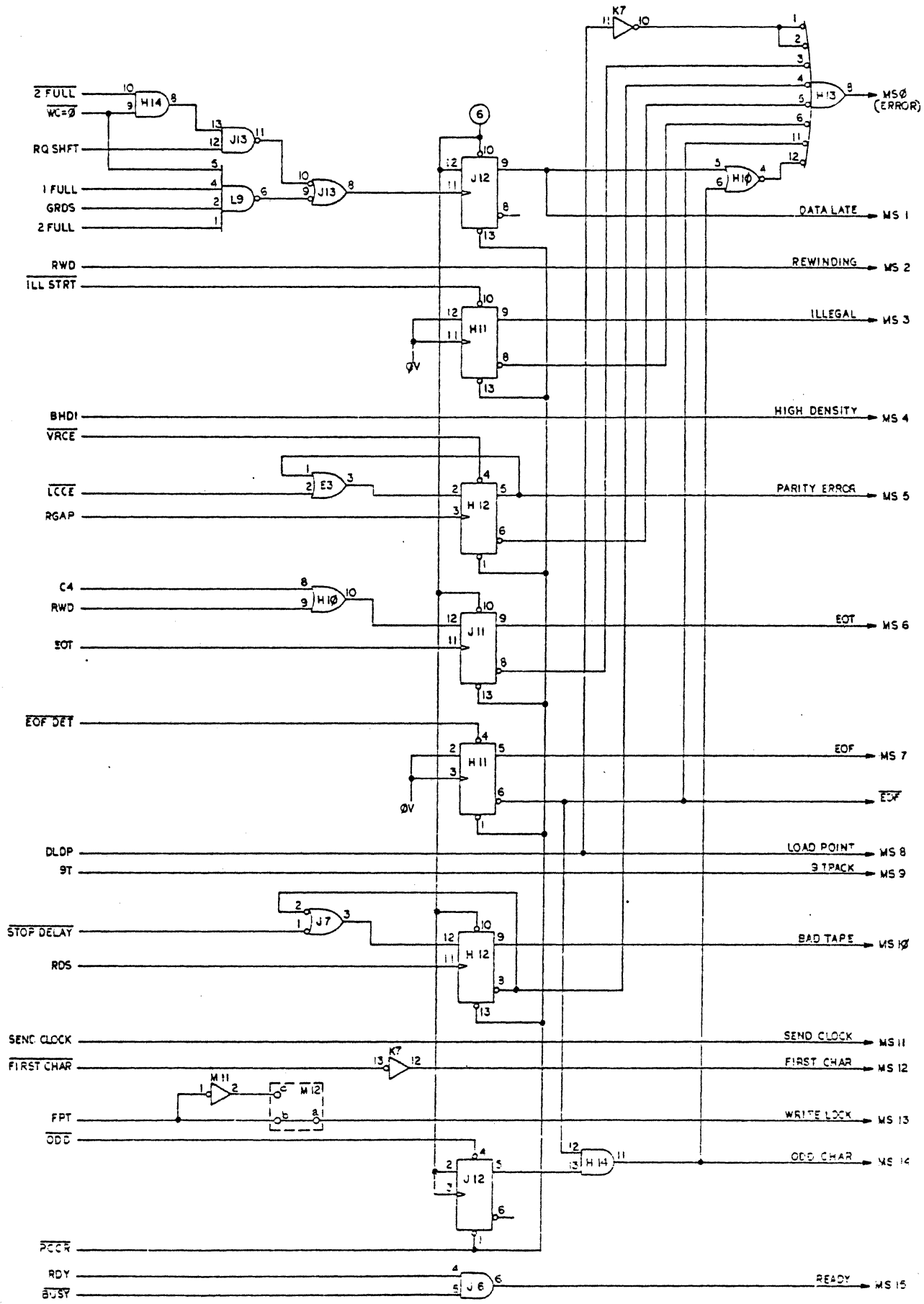
EVEN NUMBER PINS ON CONNECTOR 01 ARE SIGNAL RETURN GROUND (ØV)


RD7
RD6
RD5
RD4
RD3
RD2
RD1
9T
RDØ
THREE
RD/WRT SHFT
BCLR
RDST
XFR1-2
SER IN
M5
74165
CLK
INH
S/L
QH
ØV
L3
7451
L4
L5
F6
C9
74164
CLR
QH
QG
QF
QE
QD
QC
QB
QA
C1Ø
74ØØ
1G
2G
1D1
1D2
2D2
2D1
2D3
2D4
1D4
1D3
1Q1
1Q2
2Q2
2Q1
2Q3
2Q4
1Q4
1Q3
MD Ø
MD 1
MD 2
MD 3
MD 4
MD 5
MD 6
MD 7
E9
74164
E1Ø
74ØØ
MD 8
MD 9
MD 1Ø
MD 11
MD12
MD13
MD14
MD15

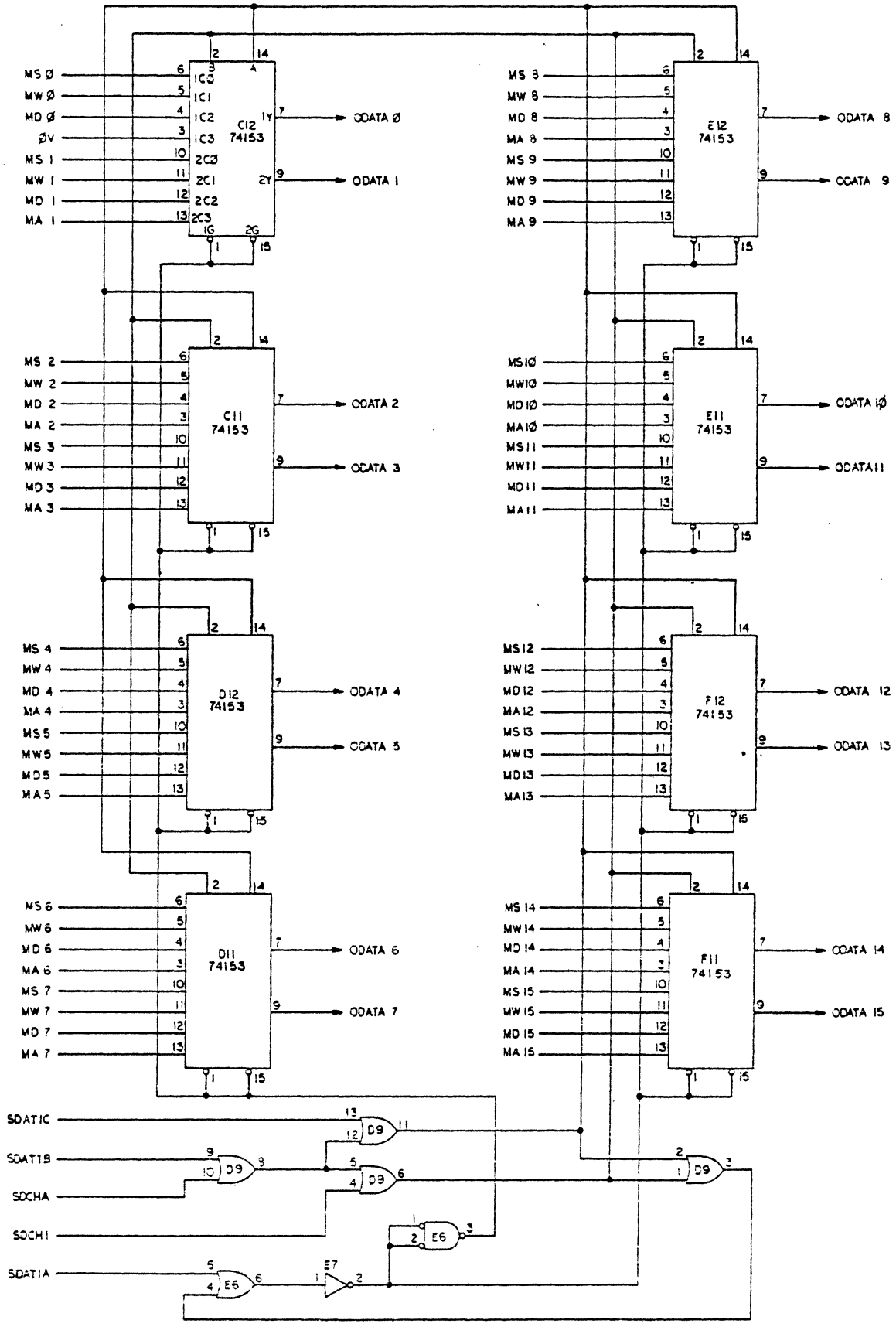

VCC
R39
C35
DENSITY LOW
H10
H8
74123
9T
9
BHDI
BHDI
H9
VCC
R38
C36
ENABLED RDS
H9
H8
74123
K6
FIRST CHAR
9
K8
EOR
J8
J8
K8
EOR2
EOR 2
EOR 2
MA0
J9
H9
VCC
R47
C41
J10
74123
5
R46
1K
F8
.022 μF
C47
0V
K10
RGAP
R35
1K
F9
.01 μF
C31
0V
H9
DELD RGAP
BCLR
K10
CRC REG RST
DRIVE SPEED SELECTION COMPONENTS



EOF/VERTICAL PARITY DETECTION LOGIC



STATUS REGISTER	
96-0004214-1	30 OF 31



DATA MULTIPLEXERS	
98-02042.14-1	31 OF 31

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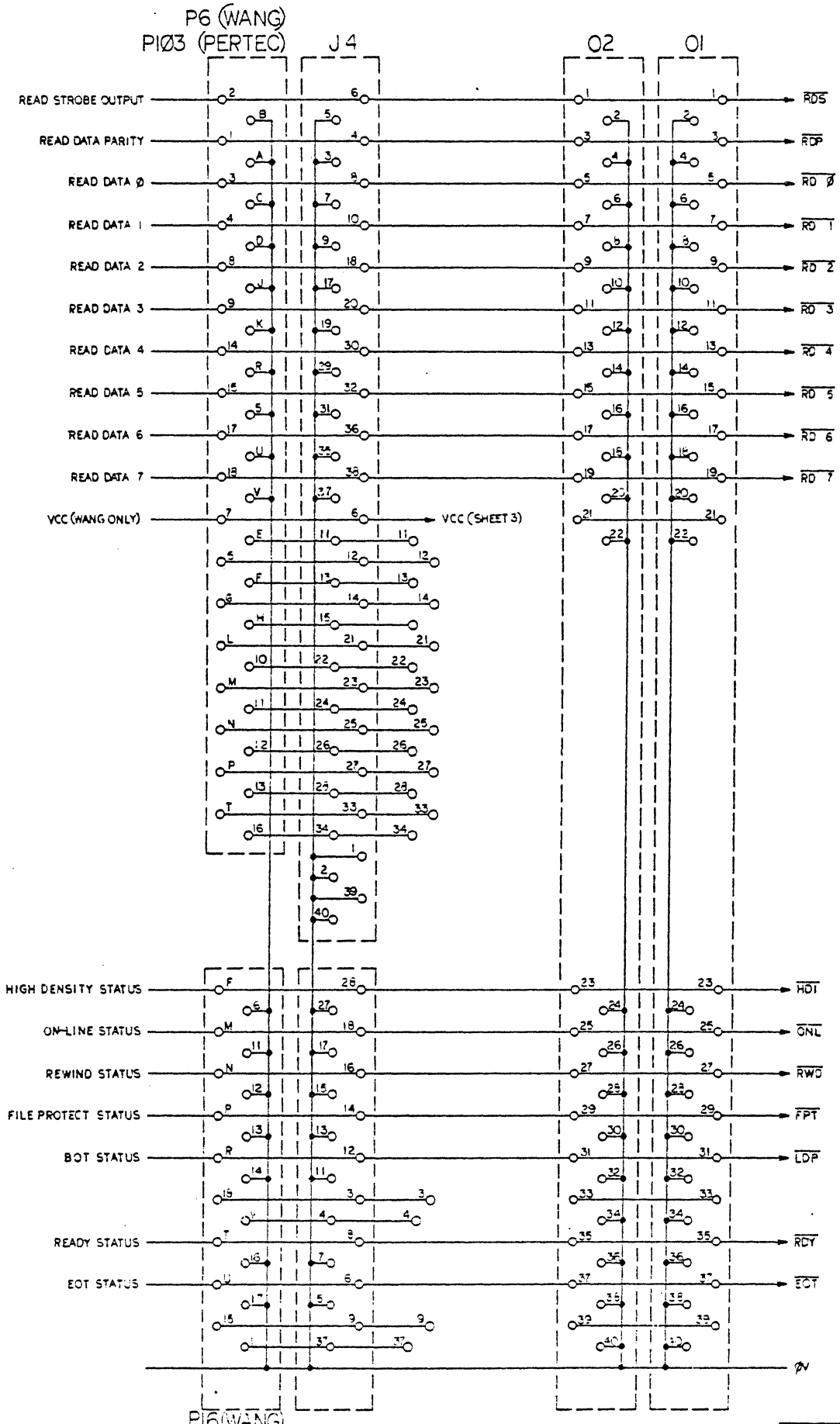
LTR	DESCRIPTION		
A	DOCUMENTATION RELEASE E.O. 1253	2/11/75	DJC
B	REF E.O 1488	10-14-75	DJC

SHEET TITLE

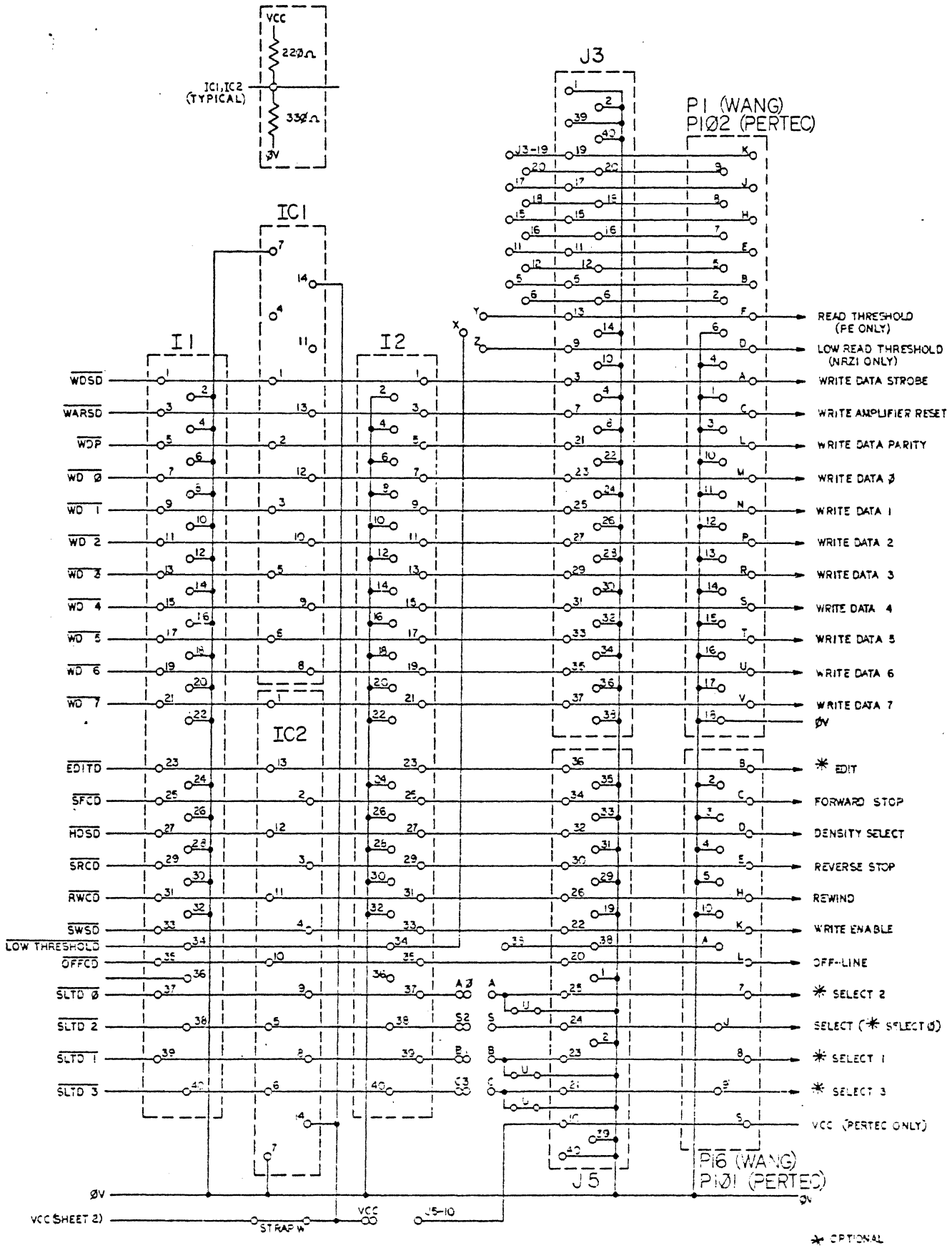
2. I/O ADAPTER - CONTROLLER INPUT
3. I/O ADAPTER - CONTROLLER OUTPUT

DWG NO 96-0204252-5 B

91-0202352-0	UNIT 3120 and 3180	Ball Computer Products, Inc. OAKLAND, CA 94618	
	DRAWN LINDSTEDT 2/75	SCHEMATIC I/O ADAPTER	
	CHECK S. SMITH 2/75		
	DESIGN		
	APP BY DJC 2/75	SIZE C DWG NO. 96-0204252-5	REV B
REF. DOCUMENTATION	APP BY	SCALE	RELEASE DATE 2-11-75 SH 1/3



I/O ADAPTER-CONTROLLER INPUT	
96-0204252-5	2 OF 3



I/O ADAPTER-CONTROLLER OUTPUT	
96-0204232-5	3 OF 3

APPENDICES

APPENDIX A
WANGCO MOD 10 INTERFACE

A.1 CABLE INTERFACE

Interface to the Wangco Mod 10 NRZI drive requires connecting the three cables originating from the I/O adapter assembly to their corresponding connectors within the drive and installing the terminator boards on the drive input signals. As shown in Figure A-1, the interface cables from the I/O adapter are designated J3, J4, and J5. The remaining ends of these cables are fitted with mating connectors compatible with the Wangco drive.

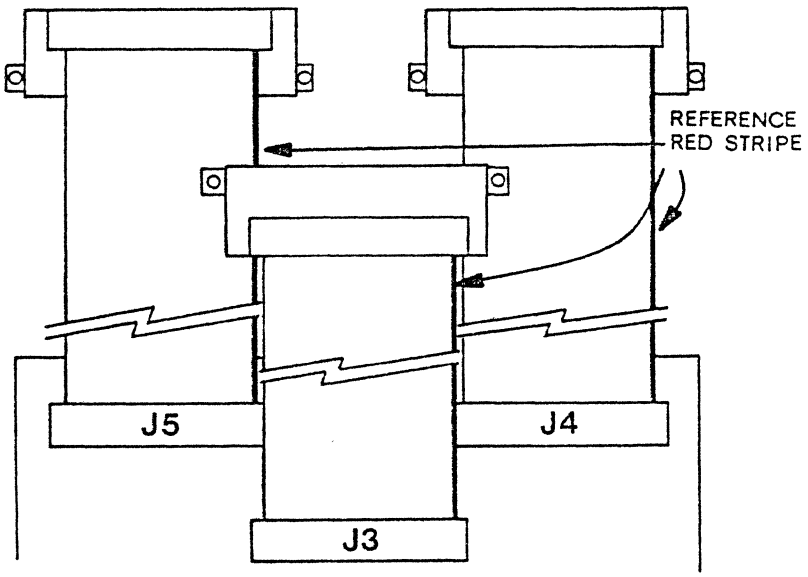


FIGURE A-1
I/O ADAPTER ASSEMBLY

Referring to Figure A-2, there are three sets of drive interface connectors. These connectors are designated J1 (A and B), J6 (A and B) and J16 (A and B). Each set is electrically indentical, permitting the corresponding cable from the adapter to be installed on either the "A" or "B" connector. Referring to the following table, interface the cables from the I/O adapter to the tape drive as noted, orienting the reference red stripe of each cable as shown in Figure A-2.

TABLE A-1

ADAPTER-TO-DRIVE CABLE INTERFACE

I/O ADAPTER CABLE DESIGNATION	DRIVE CONNECTOR	FUNCTION
J3	J1(A or B)	Write Data
J4	J6(A or B)	Read Data
J5	J16(A or B)	Drive control and Status

NOTE

Pin A on the back (circuit) side of each mating connector pc board is hand-lettered and aligns with pin A of the corresponding drive connector when correctly installed.

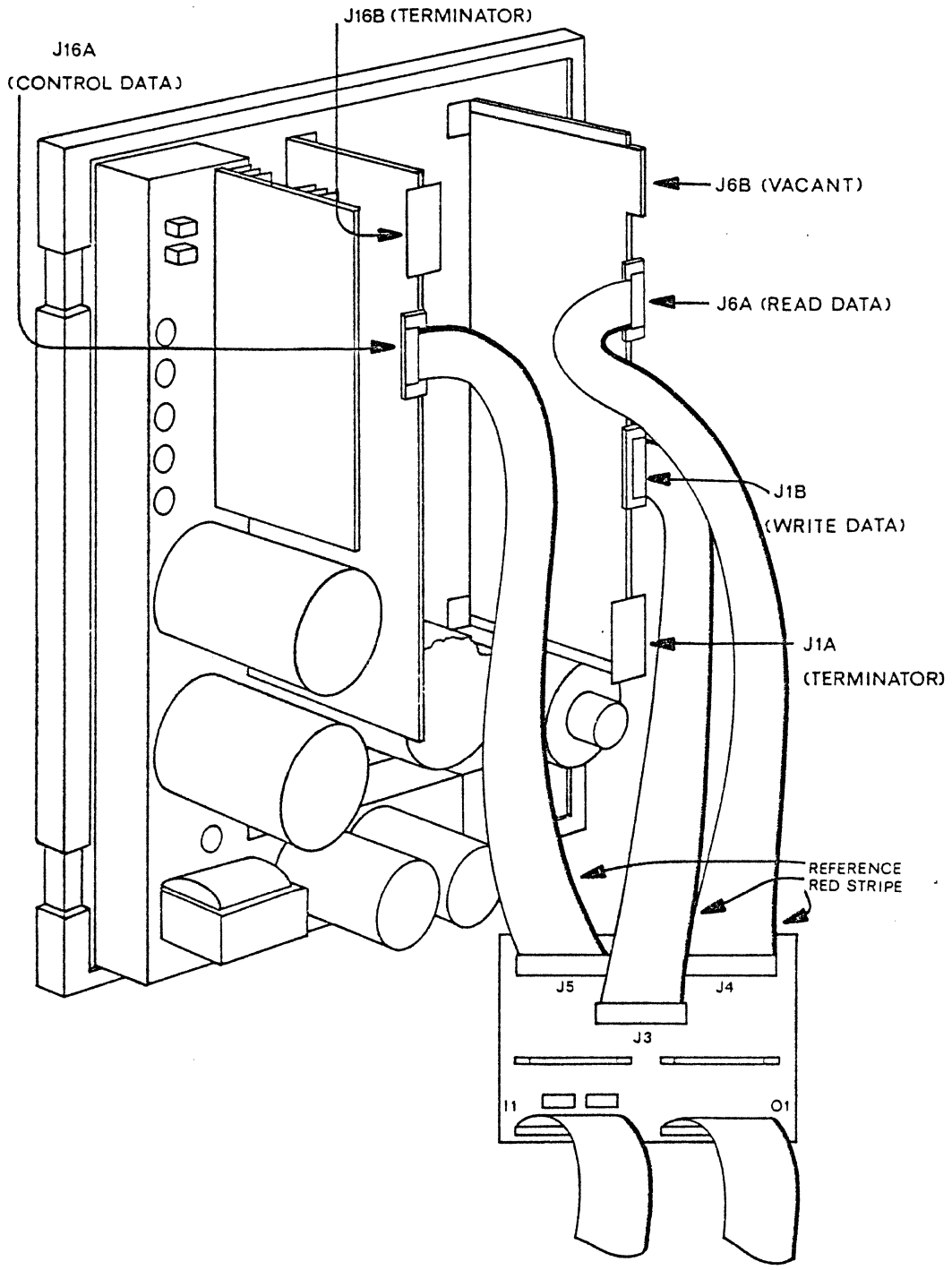


FIGURE A-2
MOD 10 DRIVE CABLE INTERFACE

A.2 TERMINATORS

If only one drive is to be interfaced to the controller, ensure that the Wangco terminator boards (supplied with the drive) are installed only on the unused connector locations at J1 and J16. The terminator boards are unique and can be identified by the part numbers etched on the circuit-side of the board. The terminator board at connector J16 (A or B) is designated 200716 while the board at connector J1 (A or B) is designated 200713. These boards are keyed to prevent incorrect installation.

NOTE

The unused connector at J6 is not terminated. These lines (read data) are terminated on the controller logic card.

If more than one drive is to be interfaced (daisy-chained) to the controller, terminator boards are installed (at J1 and J16) on only one drive.

When the adapter card termination networks are to be used in place of the drive terminator boards, remove the terminator boards from all drives and install resistor packages (Beckman 899-5-R220/330 or equivalent at locations IC1 and IC2 on the I/O adapter assembly.

A.3 DRIVE OPTIONS

If the drive incorporates the remote unit select switch option, the drive select matrix on the I/O adapter assembly must be modified. Referring to Figure A-3, install insulated jumpers between pads A(0) and S, B(1) and B, C(3) and C, and S(2) and A as shown to enable drive (unit) number assignment from the remote switch.

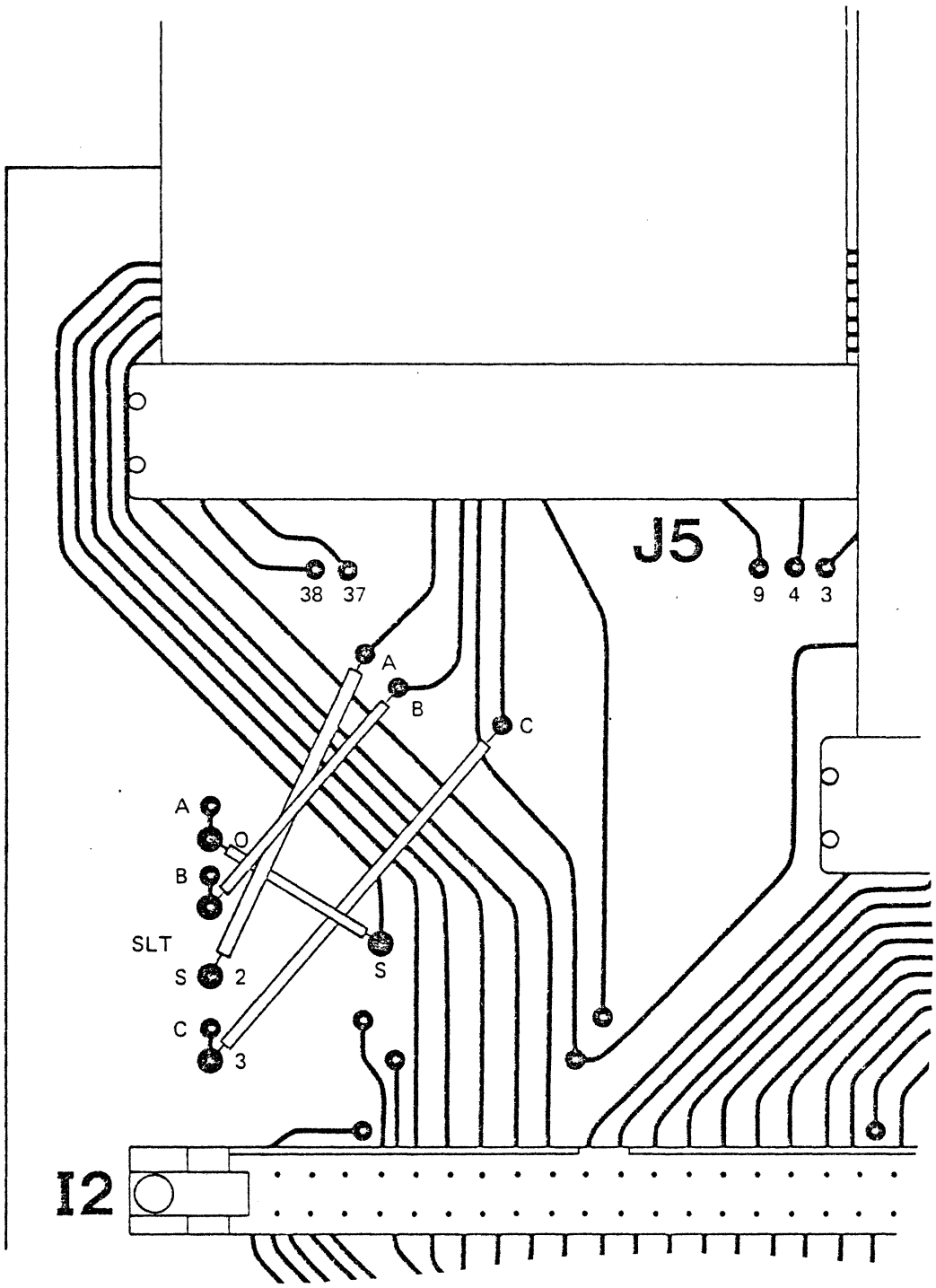


FIGURE A-3
UNIT SELECT SWITCH STRAPPING

APPENDIX B
WANGCO MOD 7/8 AND MOD 8B INTERFACE

B.1 CABLE INTERFACE

Interface to either the Wangco Mod 7/8 or Mod 8B drives requires connecting the three cables originating from the I/O adapter assembly to their corresponding connectors within the drive. As shown in Figure B-1, the drive interface cables from the I/O adapter are designated J3, J4 and J5. The remaining ends of these cables are fitted with mating connectors compatible with the Wangco drives.

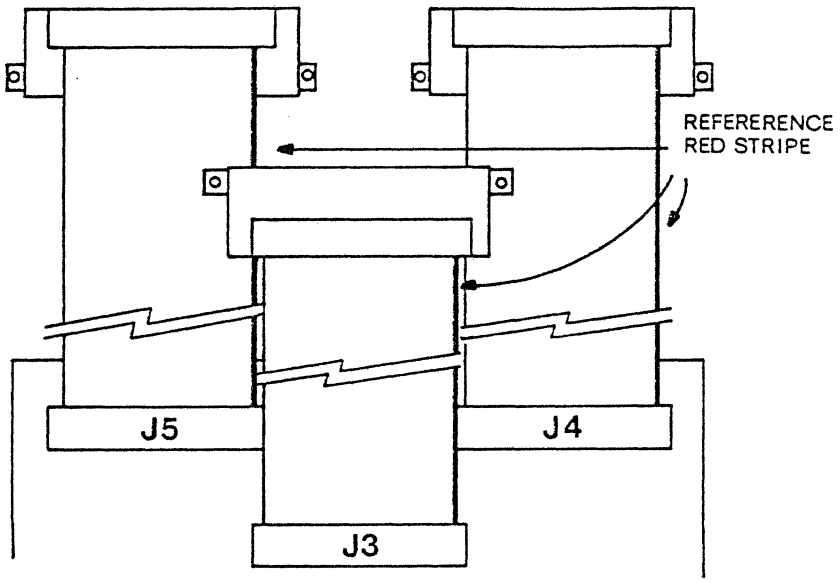


FIGURE B-1
I/O ADAPTER ASSEMBLY

As shown in Figure B-2 (Mod 7/8) and Figure B-3 (Mod 8B), there are three drive interface connectors designated J1, J6 and J16. Referring to the following table (Table B-1), install the cables from the I/O adapter to the tape drive as noted, orienting the reference red stripe of each cable as shown in the corresponding illustration.

TABLE B-1

ADAPTER-TO-DRIVE CABLE INTERFACE		
I/O ADAPTER CABLE DESIGNATION	DRIVE CONNECTOR	FUNCTION
J3	J1	Write Data
J4	J6	Read Data
J5	J16	Drive Control and Status

NOTE

Pin A on the back(circuit) side of each mating connector pc board is hand-lettered and aligns with pin A of the corresponding drive connector when correctly installed.

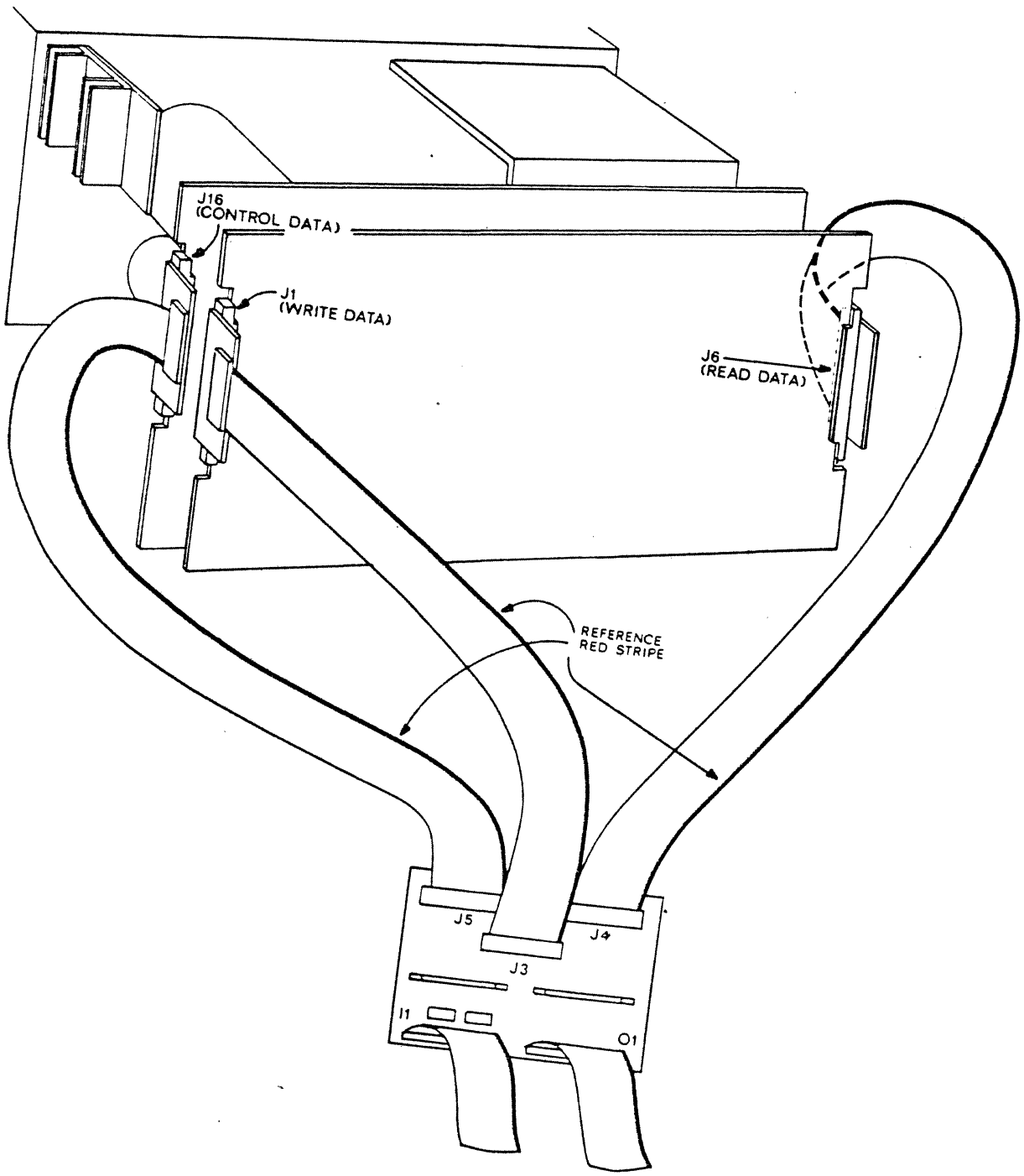


FIGURE B-2
MOD 7/8 DRIVE CABLE INTERFACE

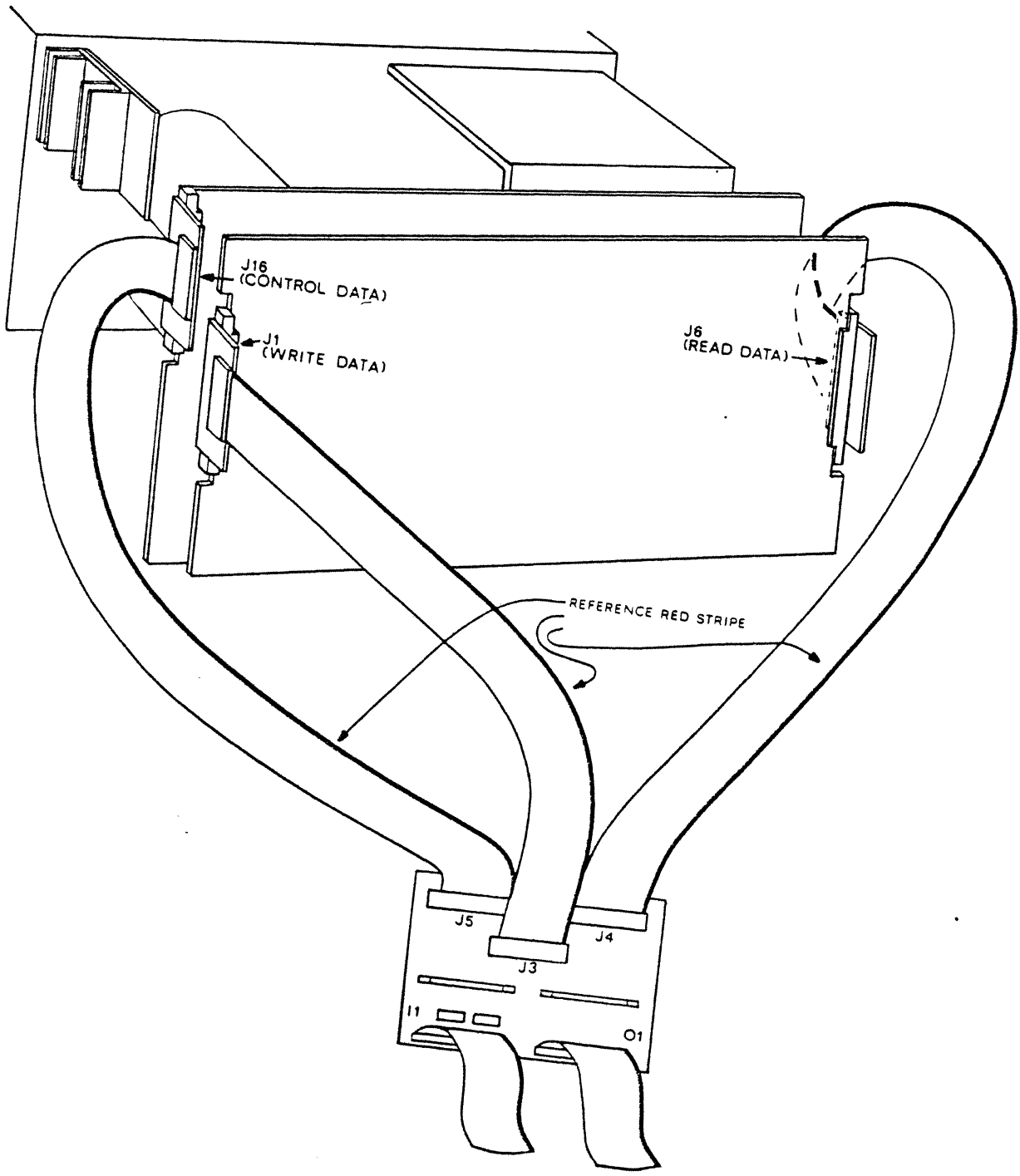


FIGURE B-3
MOD 8B DRIVE CABLE INTERFACE

B.2 SIGNAL TERMINATIONS

The tape drive provides the proper line terminations for the write data and control signals from the controller (the read data and status inputs from the drive are terminated on the controller). When only one drive is to be interfaced to the controller, all terminations are correct and no modification is required.

If more than one drive is to be interfaced (daisy-chained) to the controller, the termination resistor pairs, at the write data and control inputs, must be physically removed from all but the last drive in the chain. The write data input termination resistors are located on the drive's data electronics board near connector J1, while the control input termination resistors are located on the drive's transport electronic board near connector J16. Referring to the appropriate schematic and assembly drawings in the tape drive manual, carefully clip out the 220/330 ohm resistor pairs from the following output signal lines.

DATA ELECTRONICS BOARD

CONTROLLER SIGNAL NOMENCLATURE	*DRIVE SIGNAL NOMENCLATURE	INPUT PIN
WRITE DATA STROBE	WRITE STROBE	J1-A
LOW READ THRESHOLD	LOW CLIP SELECT	J1-D
WRITE AMPLIFIER RESET	WRITE RESET	J1-C
WRITE DATA PARITY	TRK P (TRK C)	J1-L
WRITE DATA Ø	TRK Ø	J1-M
WRITE DATA 1	TRK 1	J1-N
WRITE DATA 2	TRK 2 (TRK B)	J1-P
WRITE DATA 3	TRK 3 (TRK A)	J1-R
WRITE DATA 4	TRK 4 (TRK 8)	J1-S
WRITE DATA 5	TRK 5 (TRK 4)	J1-T
WRITE DATA 6	TRK 6 (TRK 2)	J1-U
WRITE DATA 7	TRK 7 (TRK 1)	J1-V

* Drive signal names in parentheses refer to seven-track drive configuration.

TRANSPORT ELECTRONICS BOARD		
CONTROLLER SIGNAL NOMENCLATURE	DRIVE SIGNAL NOMENCLATURE	INPUT PIN
DENSITY SELECT	DENSITY SELECT	J16-D
OFF-LINE	OFF LINE	J16-L
FORWARD STOP	FWD/STOP	J16-C
WRITE ENABLE	WRITE/ENABLE	J16-K
REVERSE STOP	REV/STOP	J16-E
REWIND	REWIND	J16-H

The I/O adapter assembly includes provision for the installation of termination resistors directly on the adapter card, allowing the termination resistors to be removed from all drives in the system. This feature eliminates the necessity of replacing the drive termination resistors in another drive when the terminated drive is either removed from the system or is powered down. Referring to the following illustration (Figure B-4), install Beckman 899-5-R220/330 (or equivalent) resistive networks in integrated circuit sockets IC1 and IC2 on the adapter assembly of the last drive only.

CAUTION

Placing termination resistors in parallel may destroy the open-collector drivers on the controller.

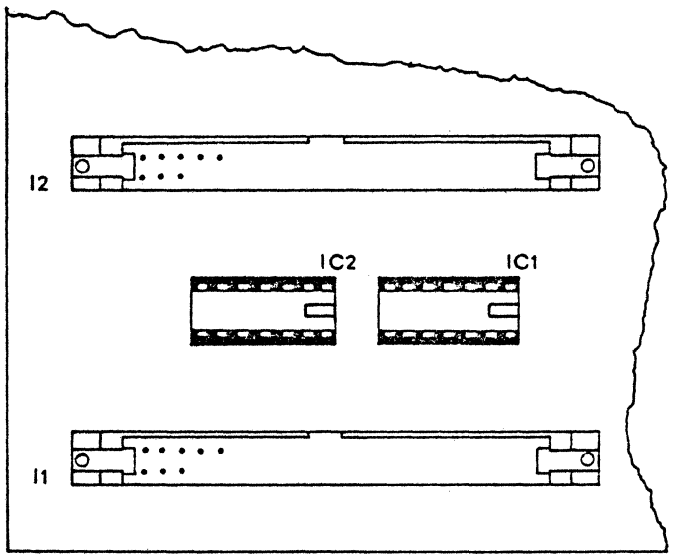


FIGURE B-4
RESISTIVE NETWORK INSTALLATION

B.3 DRIVE OPTIONS

If the drive incorporates the remote unit select option, the drive select matrix on the I/O adapter assembly must be modified. Referring to Figure B-5, install insulated jumpers between pads A(Ø) and S, B(1) and B, C(3) and C and S(2) and A as shown to enable drive (unit) number assignment from the remote switch.

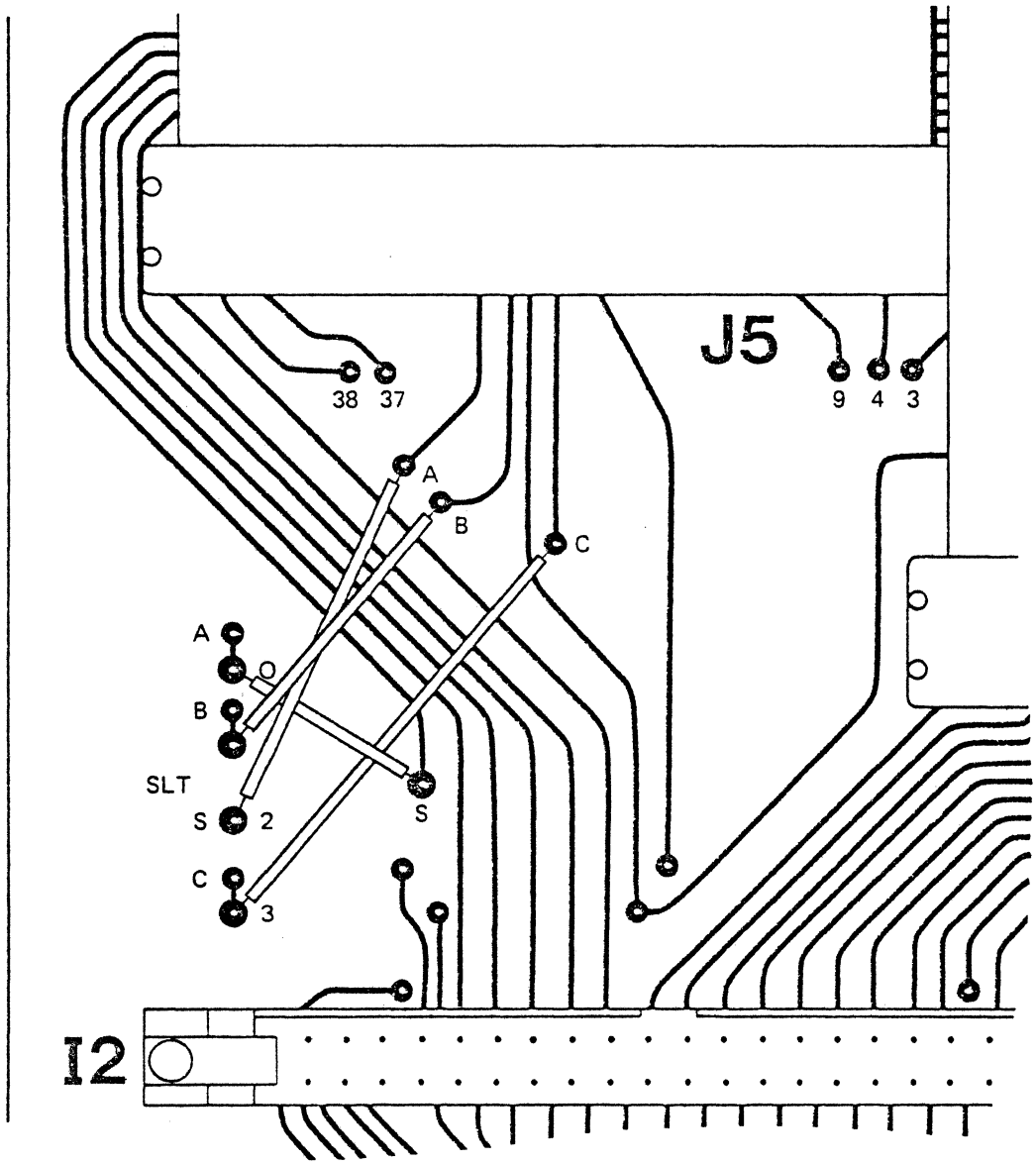


FIGURE B-5
UNIT SELECT SWITCH STRAPPING

ADDENDUM

3180/20 OPTION INTERFACE

The 3180/20 Option consists of a 3120 NRZI Controller and a 3180 PE Controller interfaced to the drive(s) on a common bus. A special controller-to adapter cable interface is supplied which connects both controllers to a single I/O adapter assembly.

Insert the 3120 logic card into the selected I/O slot as described in the 3120 Tape Controller Technical Manual. The 3120 Controller should occupy the lower of the two selected slots. Prior to installing the 3180 Controller, refer to the following table and remove the 220/330 ohm termination resistor pairs at the inputs to the deskewing buffers (READ DATA) and at the status inputs to the status command decoder logic.

NOTE

> Ensure that the data channel and interrupt priorities are maintained on the CPU back panel if a vacant slot or slots exist between the two controllers (see Section 2.5.1 in the 3120 Tape Controller Technical Manual).

Referring to the illustration on page 3 of this addendum, connect the cable assembly as shown. The individual cable mating connectors are labled with their corresponding pc card connectors.

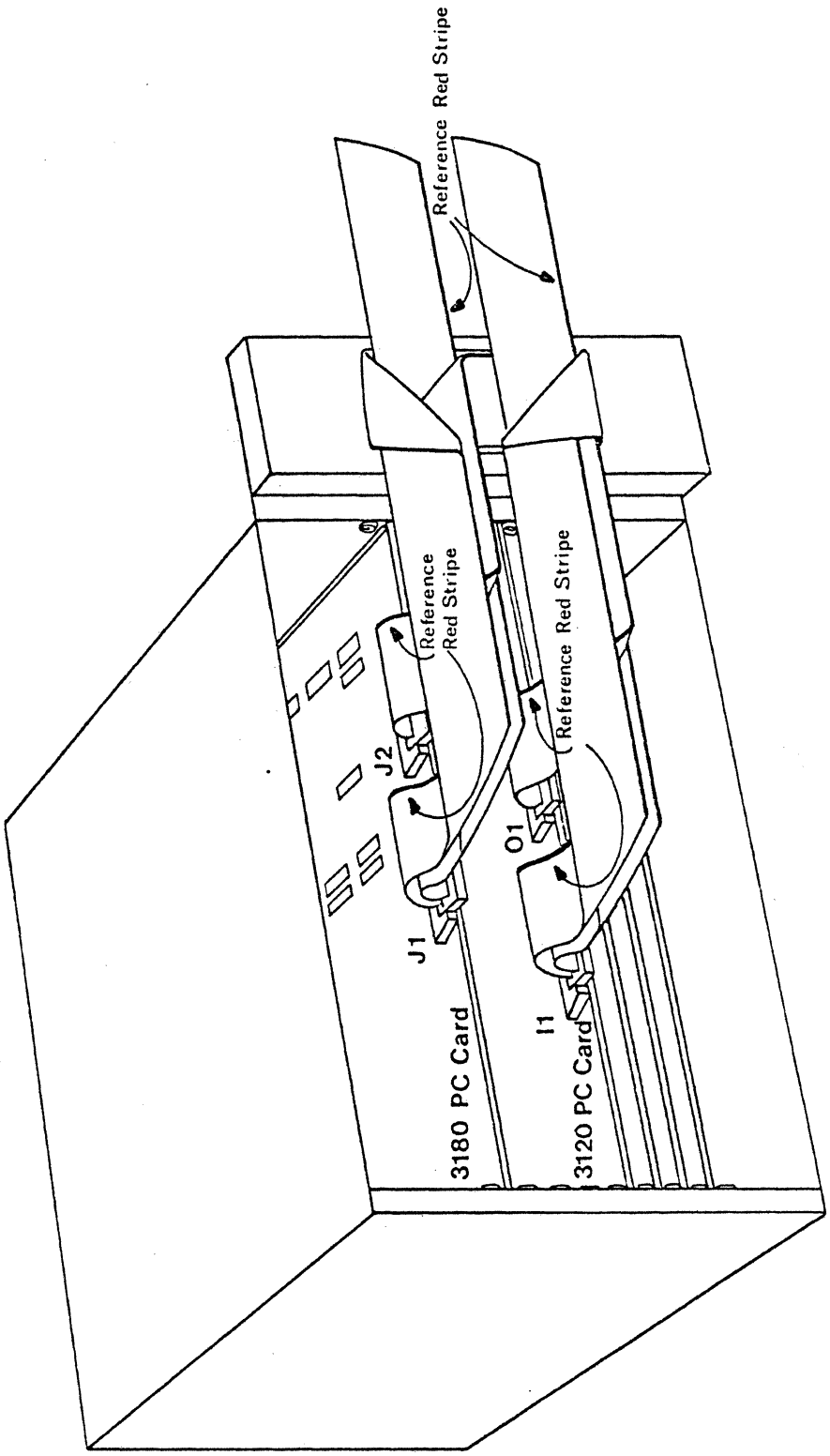
On the back panel of the CPU, install a wire-wrap jumper from pin A61 of the I/O slot occupied by the 3120 Controller to pin A61 of the I/O slot occupied by the 3180 Controller.

3180 PC CARD

RESISTOR REMOVAL

RESISTOR PAIR	SIGNAL NOMENCLATURE	PC CARD COORDINATES
R19,R20	READ DATA P	Z5
R21,R22	READ DATA Ø	R5
R23,R24	READ DATA 1	R15
R25,R26	READ DATA 2	R15
R27,R28	READ DATA 3	V11
R39,R40	READ DATA 4	N7
R31,R32	READ DATA 5	Z3
R33,R34	READ DATA 6	U3
R35,R36	READ DATA 7	Z4
R45,R46	REWIND STATUS	P15
R47,R48	FILE PROTECT STATUS	P15
R49,*R50	BOT STATUS	M13,M15
R51,R52	READY STATUS	P15
R53,R54	EOT STATUS	P15

*Resistor R50 on the schematic has been incorrectly labeled R5 on the PC card silkscreen.



3180/20 CONTROLLER-TO-ADAPTER

INTERFACE CABLE ASSEMBLY